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MS-7613 Ver: 10

uATX(244mm X 244mm)

CPU:

INTEL -Clarkdale/Lynnfied LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH

OnBoard Chipset:

Clock Gen:Silego SLG8SP585

HD Audio Codec:ALC888S

LAN:RTL8111DL 10/100/1000

IO: Fintek F71858D

Flash ROM: 32 Mb SPI (CHIP) Fire wire: VIA VT6315N

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 3

Mini PCI Express (X1) Slot * 1

ONFI Slot *1

PWM:

Controller:Intersil ISL6333 3-Phase -- 95W

Other:

SATA(SATA2-300MB/s) *6

USB2.0 *14 (Rear*6 / Front*8)

on BOARD BUZZER

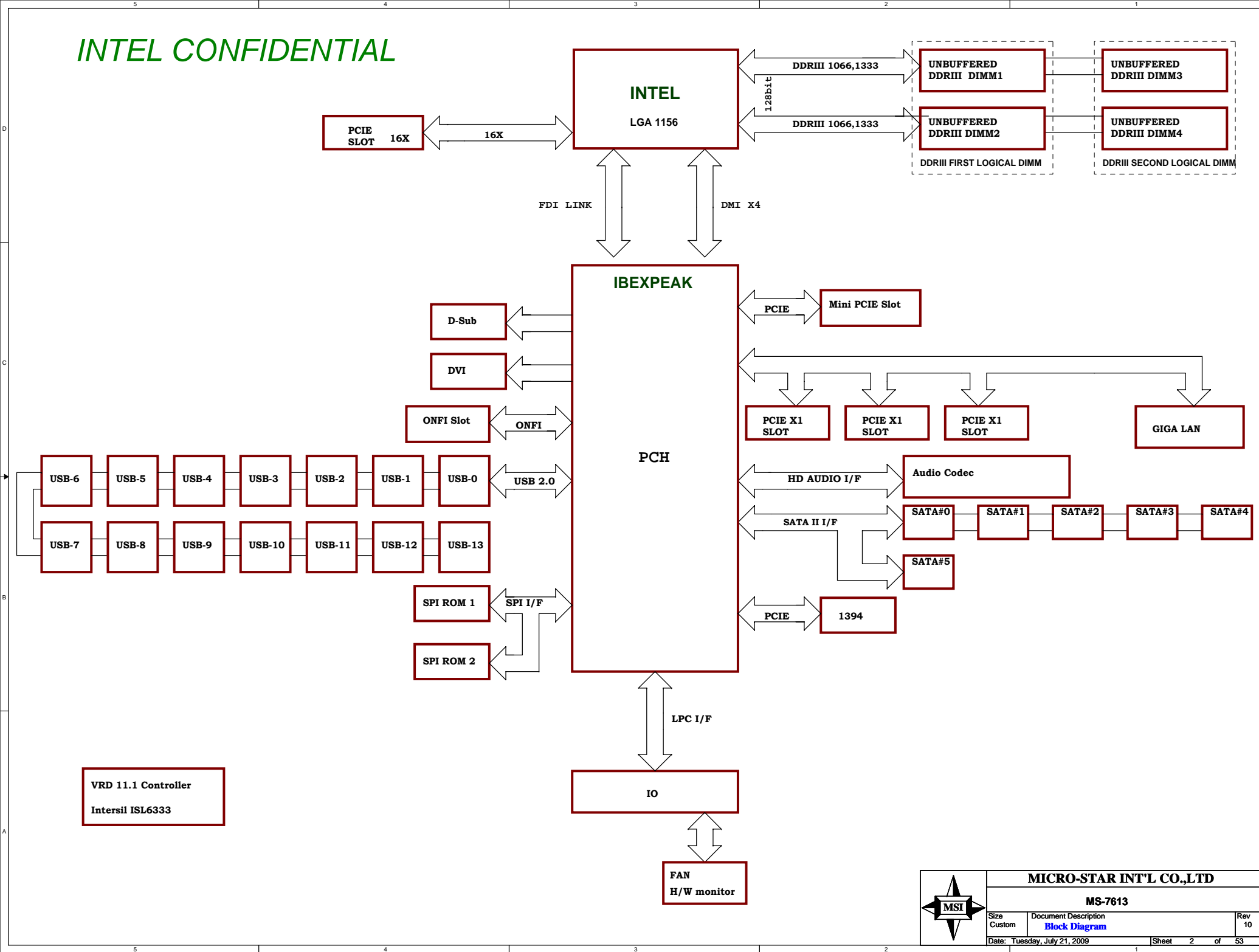
D-SUB *1

DVI PORT*1



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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100001B	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 4 CH-B	10100011B	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

TABLE 9↓
USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #2	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes



				18BXPSAK GPIO DEFINITION	
GPIO	POWER	IO	Function	Implementation	Mother board Function
GPIO0	MAIN	1	BMBUSY#	10 K Pull-up to +3.3V	ADPT_ID_DET#
GPIO1	MAIN	1	TACH1	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH1
GPIO2	MAIN	1	PCLIRQB#	See PCA Spec	PCI Interrupt E#
GPIO3	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt F#
GPIO4	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt G#
GPIO5	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt H#
GPIO6	MAIN	1	TACH2	Pull-up to +3.3V and connect to P52 pin 12. The COMM 8 assembly connects pin 12 directly to GND	COMM_8_DET#/ MOM_TH_ALRT#
GPIO7	MAIN	1	TACH3	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH3(PSU Fan Control)
GPIO8	RESUMB	0	ICG_B#		Reserved
GPIO9	RESUMB	1	OC5	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO10	RESUMB	1	OC6	10K Pull-up to +3.3V and connect to P126-pin 16	PRNTR_DET#
GPIO11	RESUMB	1	SMBALERT#	20K Pull-up to +3.3VSB. It is always enabled as a wake event.	SMBALERT#
GPIO12	RESUMB	1	LAN_DISABLE	Follow implementation in Intel P100ton Design Guide	LAN_DISABLE#
GPIO13	RESUMB	1	IO_PMB	10K Pull-up to +3.3V and connect to P151-pin 10; also add a no-installed pull-down to the net.	RDYBST_DET# or DASH SMI
GPIO14	RESUMB	1	OC7	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation. 8.2K Pull-up to +3.3V and connect to the SMI pin on the SIO	SMI# from SIO
GPIO15	RESUMB	1	PCB_GP15		Reserved
GPIO16	RESUMB	0	SATA2DP	10 M pull-up to VBAT and connect to CPU SKTOCC#, SIO pin48 and PCH	CPU_MISSING
GPIO17	MAIN	1	TACH0	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH0(Front Chassis Fan)
GPIO18	MAIN	1	PCIECLKQ#	Through a 1KΩ series resistor, 8.2K pull-up to +3.3V and connect to E15-pin 1. E15 Pin 2 connect to GND	BOOT_BLK_REC#
GPIO19	MAIN	1	SATA1DP	connect to a test point	unused
GPIO20	MAIN	1	PCIECLKRQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to HANKSVILLE -pin48	PCIECLKRQ2#
GPIO21	MAIN	1	SATA2DP	10K pull-up to +3.3V and connect to P23-pin 4.	FRNT_AUD_DET#
GPIO22	MAIN	1	SCLOCK	10K Pull-up to +3.3V and connect to P160-pin 10	INT_USB_DET#
GPIO23	MAIN	1	LDRO#	connect to a test point.	PEG_MOM_DET#
GPIO24	RESUMB	0	MBALED	Through a 1kΩ series resistor, 8.2K pull-up to +3.3V and connect to P125-Pin 1. 1M pull-up to VBAT and connect to P125-pin 3	HOOD_SW_DET#
GPIO25	RESUMB	1	PCIECLKRQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKRQ3#
GPIO26	RESUMB	1	PCIECLKRQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKRQ4#
GPIO27	RESUMB	0	OD_PLL_VR_EN	10K pull-up to +3.3VAUX	Reserved
GPIO28	RESUMB	0	PCB_GP28	connect to a test point	unused
GPIO29	RESUMB	0	SLP_LAN#	refer to the PCA spec.	SLP_LAN#
GPIO30	RESUMB	1	SUS_PWRACK	100K Pull-up to 3V_AUX	unused
GPIO31	MAIN	1	ACPRESENT	10K Pull-up to +3.3V and connect to P25-pin 10	FRONT_USB_DET1#
GPIO32	MAIN	0	PCB_GP32	Through a 1kΩ series resistor, 10K pull-up to +3.3V and connect to P2-pin 6.	NON-EPA_PS_DET#

GPIO33	MAIN	0	PCB_GP33	Through a 1kΩ series resistor, 8.2K pull-up to +3.3V and connect to pin 1 of jumper E1 and E1 pin2 to GND	FDT_OVRD#
GPIO34	MAIN	0	SP_PC#	3.3K Pull-down to GND and connect to P124-pin 2. Decouple P124-pin 2 with 0.1μF P124 pin 1 2.2K pull-up to 5V and P124 pin 6 2.2k pull-up to 5V	HOOD_LOCK_DET
GPIO35	MAIN	0	SATACLKREQ#	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV0
GPIO36	MAIN	1	SATA2DP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV1
GPIO37	MAIN	1	SATA3DP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID2
GPIO38	MAIN	1	SLOAD	Through a series 1K resistor, 10K Pull-up to +3.3V and 10K pull-down to GND and connect to P5-pin 9. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID0
GPIO39	MAIN	1	SDATAOUT0	Pull-up to +3.3V and connect to top-layer ring of PCA mounting hole used for SFF Basepan detect feature.	BRD_ID1
GPIO40	RESUMB	1	OC1	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for XDP implementation. 8.2kΩ pull-down to GND and connect to E49-pin 2 E49 pin-1 300 pull-up to +3.3V	PASSWORD_EN
GPIO41	RESUMB	1	OC2	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO42	RESUMB	1	OC3	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO43	RESUMB	1	OC4	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO44	RESUMB	1	PCIECLKRQ#	10K pull-up to +3.3VAUX and connect to a test point.	PCIECLKRQ6#
GPIO45	RESUMB	1	PCIECLKRQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to J3-pin8 J7	PRSN#_J31
GPIO46	RESUMB	1	PCIECLKRQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKRQ7#
GPIO47	RESUMB	1	PBG_A_CLKRQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to J4-pin848 and B81	PRSN#_J41
GPIO48	MAIN	1	SDATAOUT1	Through a series 1K resistor, 10K Pull-up to +3.3V and 10K pull-down to GND and connect to P5-pin 10. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID1
GPIO49	MAIN	0	SATA3DP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID0
GPIO50	MAIN	1	PCLRBQ#1	8.2k pull-up to VCC3	REQ1#
GPIO51	MAIN	0	PCLQNT#1	connect to a test point	GNT1#
GPIO52	MAIN	1	PCLRBQ#2	8.2k pull-up to VCC3	REQ2#
GPIO53	MAIN	0	PCLQNT#2	connect to a test point	GNT2#
GPIO54	MAIN	1	PCLRBQ#3	Through a 8.2KΩ series resistor, connect to E14-pin 2 and 1K pull-down to GND. E14-pin1 connect to +3.3V	BOOT_BLK_EN#
GPIO55	MAIN	0	PCLQNT#3	connect to a test point	GNT3#
GPIO56	RESUMB	1	PBG_B_CLKRQ#	refer to the PCA spec.	AUD_AMP_DIS#
GPIO57	MAIN	1	PCB_GP57	10K Pull-up to +3.3VME installed and 10K pull-down to GND not installed.	TPM_PP

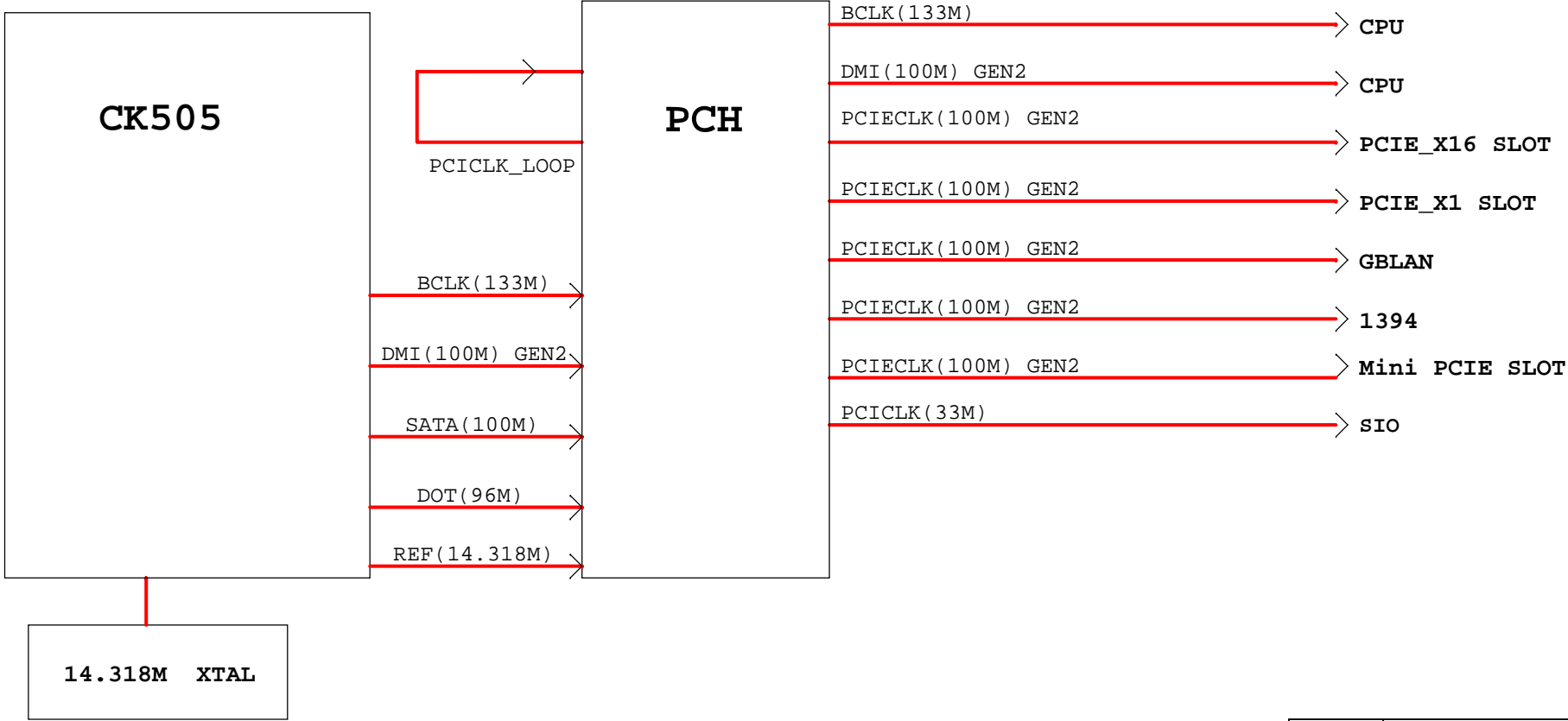
GPIO58	RESUMB	0	SMCLK	10K pull-up to 3V_AUX	SMCLK
GPIO59	RESUMB	1	OC0	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO60	RESUMB	0	SMDALBRT#	10K pull-up to 3V_AUX	SMDALARM
GPIO61	RESUMB	0	SUS_STAT#	connect to a test pin	LPCPD#
GPIO62	RESUMB	0	SUSCLK	SUSCLK to SIO-pin16	SUSCLK
GPIO63	RESUMB	0	SLP_S#	Connect to the SIO-pin37	SLP_S#
GPIO64	MAIN	0	CLKOUTFLBK0	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK0
GPIO65	MAIN	0	CLKOUTFLBK1	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK1
GPIO66	MAIN	0	CLKOUTFLBK2	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK2
GPIO67	MAIN	0	CLKOUTFLBK3	refer to the PCA spec. unused clock connect to a test point	CLK14M
GPIO72	RESUMB	1	PCB_GP72	Pull-up to +3.3V and connect to P24-pin 10	FRONT_USB_DET0#
GPIO73	RESUMB	1	PCIECLKRQ#	10K pull-up to +3.3VAUX and through a 0Ω series resistor, connect to J42-pin8 J7, B31, B48, and B81	PRSN#_J42
GPIO74	RESUMB	0	SMDALBRT#	10K pull-up to 3V_AUX	SMDALERT#
GPIO75	RESUMB	0	SMDLIDATA	10K pull-up to 3V_AUX	SMDLIDATA

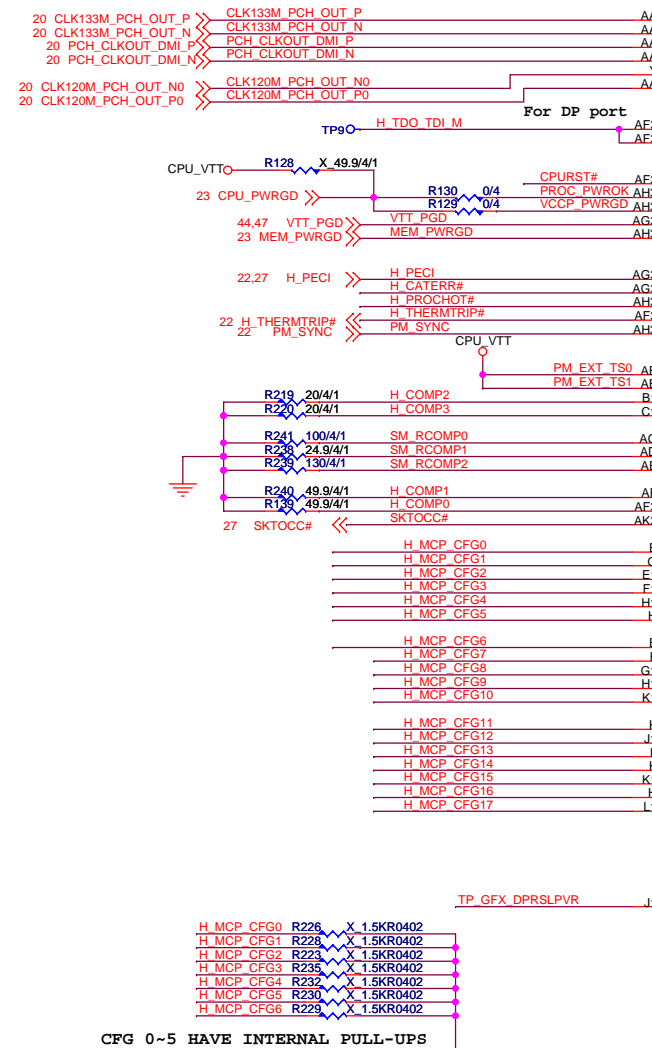


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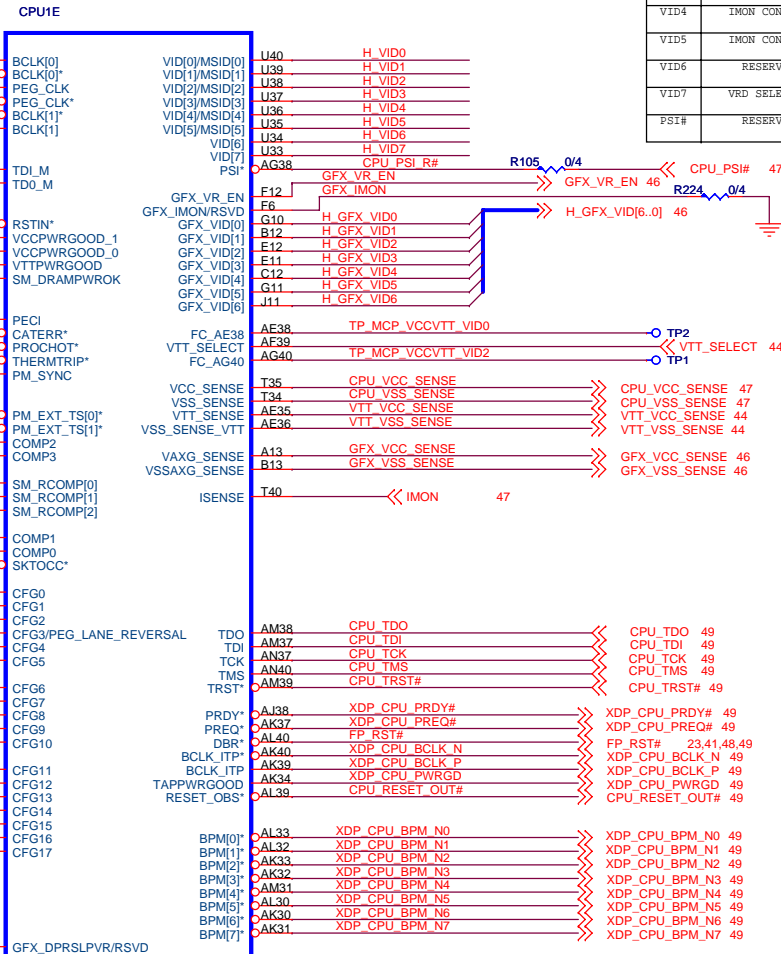
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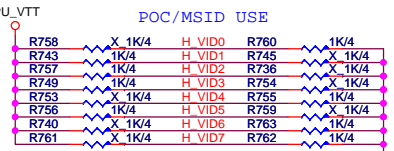
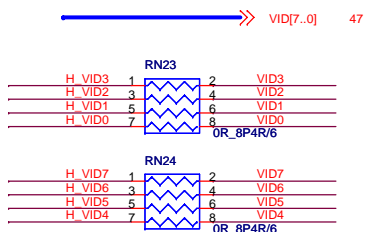


CFG	H	L	DESCRIPTION
0	SEE PEG CONFIG TABLE		PEG SEL0
1	SEE PEG CONFIG TABLE		PEG SEL1
2	SEE PEG CONFIG TABLE		PEG SEL2
3	NORM	REVERSED	PEG LANE REVERSAL
4	DISABLE	ENABLED	DP PRESENCE
5			

PEG CONFIG TABLE			
SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8



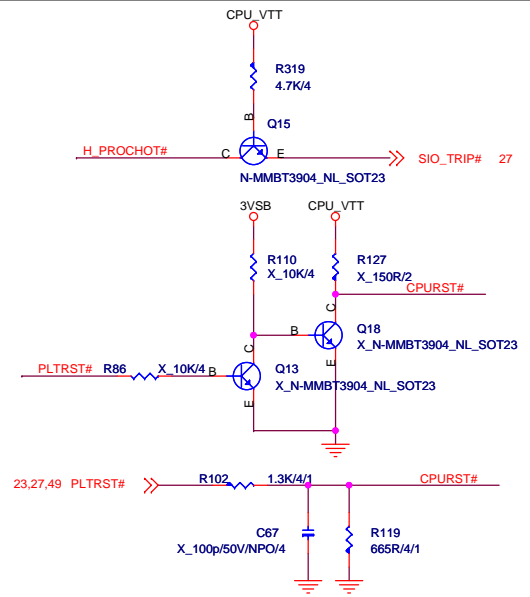
	FUNCTION	DEFAULT
VID0	MSI0	0
VID1	MSI1	1
VID2	MSI2	1
VID3	IMON CONFIG0	1
VID4	IMON CONFIG1	0
VID5	IMON CONFIG2	1
VID6	RESERVED	
VID7	VRD SELECT	LOW
PSI#	RESERVED	LOW



Market Segment Selection Truth Table for MSID[2:0]

MSID2	MSID1	MSID0	Description ¹
1	1	0	Lynnfield and Havendale processors supported ³

Processor Icc(max)	I _{MAX} Iout gain: 900 mV = I _{MAX}	POC Gain Setting
Disabled	-	000
Icc(max) ≤ 40 A	40 A	001
40 A < Icc(max) ≤ 60 A	60 A	010
60 A < Icc(max) ≤ 80 A	80 A	011
80 A < Icc(max) ≤ 100 A	100 A	100
100 A < Icc(max) ≤ 120 A	120 A	101
120 A < Icc(max) ≤ 140 A	140 A	110
140 A < Icc(max) ≤ 180 A	180 A	111



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15,16 MEM_MB_DATA[63..0] >>

15,16 MEM_MB_ADD[15..0] >>

CPU1B

15,16 MEM_MB_WE_L >> MEM_MB_WE_L AU26 SB_WE*
15,16 MEM_MB_CAS_L >> MEM_MB_CAS_L AW27 SB_CAS*
15,16 MEM_MB_RAS_L >> MEM_MB_RAS_L AW26 SB_RAS*

15,16 MEM_MB_BANK0 >> MEM_MB_BANK0 AU25 SB_BA[0]
15,16 MEM_MB_BANK1 >> MEM_MB_BANK1 AW25 SB_BA[1]
15,16 MEM_MB_BANK2 >> MEM_MB_BANK2 AV12 SB_BA[2]

15 MEM_MB_CS_L0 >> MEM_MB_CS_L0 AY27 SB_CS[0]*
15 MEM_MB_CS_L1 >> MEM_MB_CS_L1 AW29 SB_CS[1]*
16 MEM_MB_CS_L2 >> MEM_MB_CS_L2 AV26 SB_CS[2]*
16 MEM_MB_CS_L3 >> MEM_MB_CS_L3 AV29 SB_CS[3]*

15 MEM_MB_CKE0 >> MEM_MB_CKE0 AW8 SB_CKE[0]
15 MEM_MB_CKE1 >> MEM_MB_CKE1 AY9 SB_CKE[1]
16 MEM_MB_CKE2 >> MEM_MB_CKE2 AU9 SB_CKE[2]
16 MEM_MB_CKE3 >> MEM_MB_CKE3 AV9 SB_CKE[3]

15 MEM_MB_ODT0 >> MEM_MB_ODT0 AU27 SB_ODT[0]
15 MEM_MB_ODT1 >> MEM_MB_ODT1 AU29 SB_ODT[1]
16 MEM_MB_ODT2 >> MEM_MB_ODT2 AV27 SB_ODT[2]
16 MEM_MB_ODT3 >> MEM_MB_ODT3 AU28 SB_ODT[3]

15 MEM_MB_CLK_H0 >> MEM_MB_CLK_H0 AR17 SB_CK[0]
15 MEM_MB_CLK_L0 >> MEM_MB_CLK_L0 AR16 SB_CK[0]*
15 MEM_MB_CLK_H1 >> MEM_MB_CLK_H1 AT15 SB_CK[1]
15 MEM_MB_CLK_L1 >> MEM_MB_CLK_L1 AR15 SB_CK[1]*
16 MEM_MB_CLK_H2 >> MEM_MB_CLK_H2 AN17 SB_CK[2]
16 MEM_MB_CLK_L2 >> MEM_MB_CLK_L2 AN16 SB_CK[2]*
16 MEM_MB_CLK_H3 >> MEM_MB_CLK_H3 AR19 SB_CK[3]
16 MEM_MB_CLK_L3 >> MEM_MB_CLK_L3 AR18 SB_CK[3]*

AM23 SB_CS[4]*
AM24 SB_CS[5]*
AL24 SB_CS[6]*
AK24 SB_CS[7]*

AR14 SB_DQS[8]
AR13 SB_DQS[8]*

AR12 SB_ECC_CB[0]
AT13 SB_ECC_CB[1]
AN15 SB_ECC_CB[2]
AP14 SB_ECC_CB[3]
AM12 SB_ECC_CB[4]
AN12 SB_ECC_CB[5]
AN14 SB_ECC_CB[6]
AP13 SB_ECC_CB[7]

DDR_B

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SB_DQS[0] AF4 MEM_MB_DQS_H0 >> MEM_MB_DQS_H0 15,16
SB_DQS[0] AE5 MEM_MB_DQS_L0 >> MEM_MB_DQS_L0 15,16
SB_DM[0] AE4 MEM_MB_DM0 >> MEM_MB_DM0 15,16

SB_DQ[0] AD7 MEM_MB_DATA0
SB_DQ[1] AD6 MEM_MB_DATA1
SB_DQ[2] AH8 MEM_MB_DATA2
SB_DQ[3] AJ8 MEM_MB_DATA3
SB_DQ[4] AC7 MEM_MB_DATA4
SB_DQ[5] AC6 MEM_MB_DATA5
SB_DQ[6] AE5 MEM_MB_DATA6
SB_DQ[7] AE6 MEM_MB_DATA7

SB_DQS[1] AH6 MEM_MB_DQS_H1 >> MEM_MB_DQS_H1 15,16
SB_DQS[1] AJ5 MEM_MB_DQS_L1 >> MEM_MB_DQS_L1 15,16
SB_DM[1] AH4 MEM_MB_DM1 >> MEM_MB_DM1 15,16

SB_DQ[8] AG5 MEM_MB_DATA8
SB_DQ[9] AH7 MEM_MB_DATA9
SB_DQ[10] AK6 MEM_MB_DATA10
SB_DQ[11] AL4 MEM_MB_DATA11
SB_DQ[12] AG6 MEM_MB_DATA12
SB_DQ[13] AG4 MEM_MB_DATA13
SB_DQ[14] AJ7 MEM_MB_DATA14
SB_DQ[15] AK7 MEM_MB_DATA15

SB_DQS[2] AN6 MEM_MB_DQS_H2 >> MEM_MB_DQS_H2 15,16
SB_DQS[2] AM6 MEM_MB_DQS_L2 >> MEM_MB_DQS_L2 15,16
SB_DM[2] AM7 MEM_MB_DM2 >> MEM_MB_DM2 15,16

SB_DQ[16] AL6 MEM_MB_DATA16
SB_DQ[17] AN5 MEM_MB_DATA17
SB_DQ[18] AP6 MEM_MB_DATA18
SB_DQ[19] AR5 MEM_MB_DATA19
SB_DQ[20] AL5 MEM_MB_DATA20
SB_DQ[21] AM4 MEM_MB_DATA21
SB_DQ[22] AN7 MEM_MB_DATA22
SB_DQ[23] AP5 MEM_MB_DATA23

SB_DQS[3] AR8 MEM_MB_DQS_H3 >> MEM_MB_DQS_H3 15,16
SB_DQS[3] AP8 MEM_MB_DQS_L3 >> MEM_MB_DQS_L3 15,16
SB_DM[3] AT7 MEM_MB_DM3 >> MEM_MB_DM3 15,16

SB_DQ[24] AT6 MEM_MB_DATA24
SB_DQ[25] AR7 MEM_MB_DATA25
SB_DQ[26] AR9 MEM_MB_DATA26
SB_DQ[27] AM8 MEM_MB_DATA27
SB_DQ[28] AN8 MEM_MB_DATA28
SB_DQ[29] AR6 MEM_MB_DATA29
SB_DQ[30] AL8 MEM_MB_DATA30
SB_DQ[31] AT9 MEM_MB_DATA31

SB_DQS[4] AT25 MEM_MB_DQS_H4 >> MEM_MB_DQS_H4 15,16
SB_DQS[4] AR24 MEM_MB_DQS_L4 >> MEM_MB_DQS_L4 15,16
SB_DM[4] AN24 MEM_MB_DM4 >> MEM_MB_DM4 15,16

SB_DQ[32] AN23 MEM_MB_DATA32
SB_DQ[33] AP23 MEM_MB_DATA33
SB_DQ[34] AR25 MEM_MB_DATA34
SB_DQ[35] AR26 MEM_MB_DATA35
SB_DQ[36] AT23 MEM_MB_DATA36
SB_DQ[37] AP22 MEM_MB_DATA37
SB_DQ[38] AP25 MEM_MB_DATA38
SB_DQ[39] AT26 MEM_MB_DATA39

SB_DQS[5] AP32 MEM_MB_DQS_H5 >> MEM_MB_DQS_H5 15,16
SB_DQS[5] AR32 MEM_MB_DQS_L5 >> MEM_MB_DQS_L5 15,16
SB_DM[5] AN32 MEM_MB_DM5 >> MEM_MB_DM5 15,16

SB_DQ[40] AT32 MEM_MB_DATA40
SB_DQ[41] AP31 MEM_MB_DATA41
SB_DQ[42] AR33 MEM_MB_DATA42
SB_DQ[43] AM32 MEM_MB_DATA43
SB_DQ[44] AT31 MEM_MB_DATA44
SB_DQ[45] AR31 MEM_MB_DATA45
SB_DQ[46] AR34 MEM_MB_DATA46
SB_DQ[47] AT33 MEM_MB_DATA47

SB_DQS[6] AR36 MEM_MB_DQS_H6 >> MEM_MB_DQS_H6 15,16
SB_DQS[6] AR37 MEM_MB_DQS_L6 >> MEM_MB_DQS_L6 15,16
SB_DM[6] AM33 MEM_MB_DM6 >> MEM_MB_DM6 15,16

SB_DQ[48] AR35 MEM_MB_DATA48
SB_DQ[49] AT36 MEM_MB_DATA49
SB_DQ[50] AN33 MEM_MB_DATA50
SB_DQ[51] AP36 MEM_MB_DATA51
SB_DQ[52] AP34 MEM_MB_DATA52
SB_DQ[53] AT35 MEM_MB_DATA53
SB_DQ[54] AN34 MEM_MB_DATA54
SB_DQ[55] AP37 MEM_MB_DATA55

SB_DQS[7] AL37 MEM_MB_DQS_H7 >> MEM_MB_DQS_H7 15,16
SB_DQS[7] AM36 MEM_MB_DQS_L7 >> MEM_MB_DQS_L7 15,16
SB_DM[7] AK35 MEM_MB_DM7 >> MEM_MB_DM7 15,16

SB_DQ[56] AL35 MEM_MB_DATA56
SB_DQ[57] AM35 MEM_MB_DATA57
SB_DQ[58] AJ36 MEM_MB_DATA58
SB_DQ[59] AJ37 MEM_MB_DATA59
SB_DQ[60] AN35 MEM_MB_DATA60
SB_DQ[61] AM34 MEM_MB_DATA61
SB_DQ[62] AJ35 MEM_MB_DATA62
SB_DQ[63] AL36 MEM_MB_DATA63

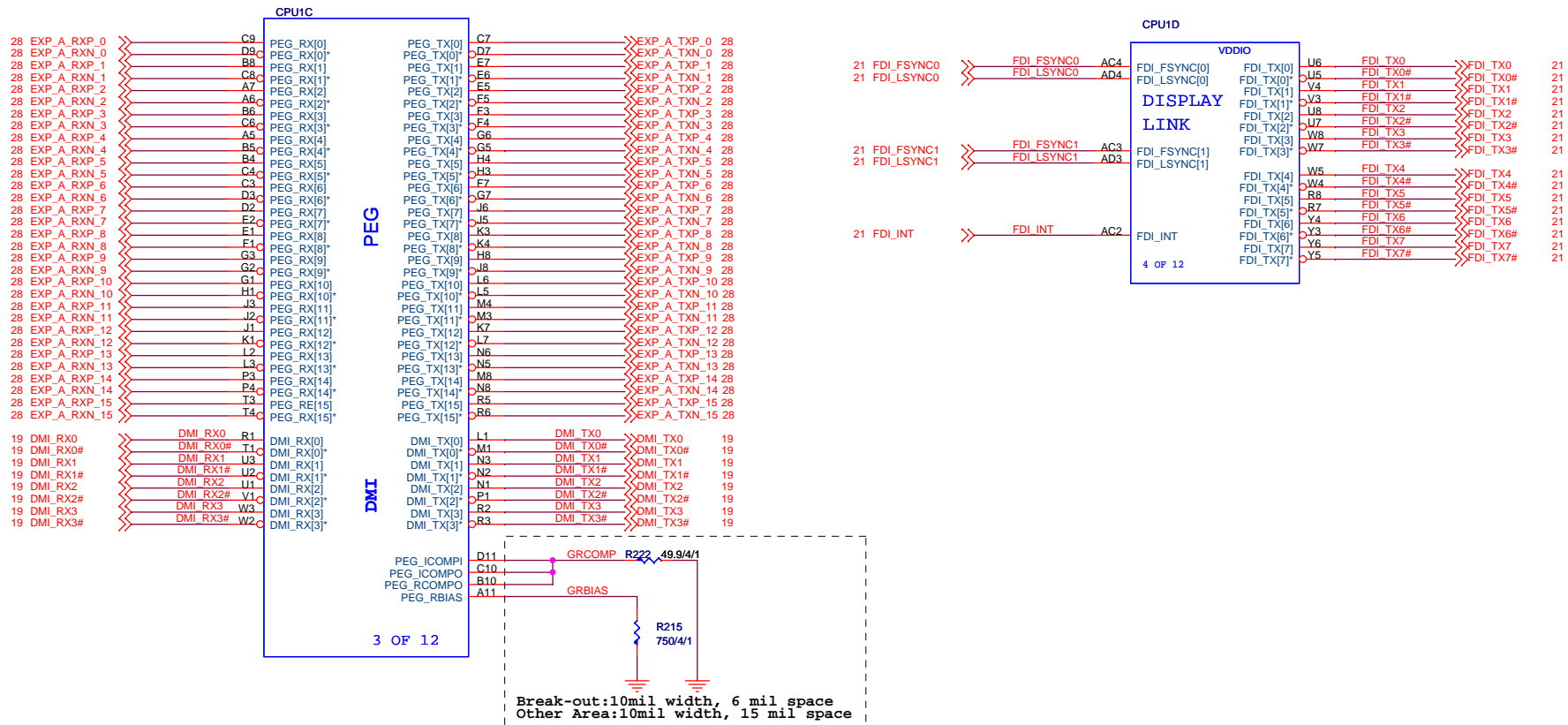


MICRO-STAR INT'L CO.,LTD

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Size Custom Document Description CPU-Memory CH-B Rev 10

Date: Tuesday, July 21, 2009 Sheet 8 of 53



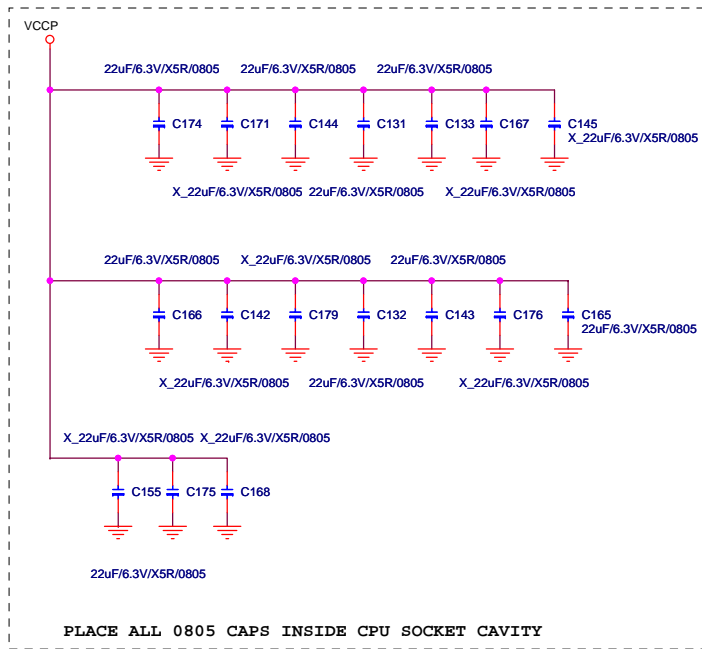
MICRO-STAR INT'L CO.,LTD

MS-7613

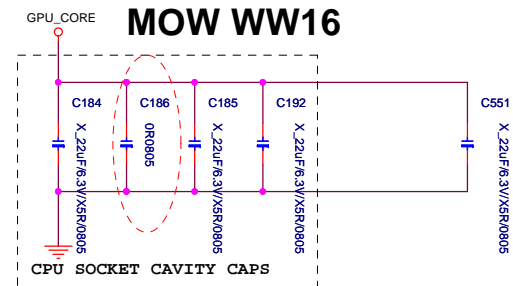
Size	Document Description	Rev
Custom	CPU-PEG/DMI	10
Date: Tuesday, July 21, 2009	Sheet 9 of 53	



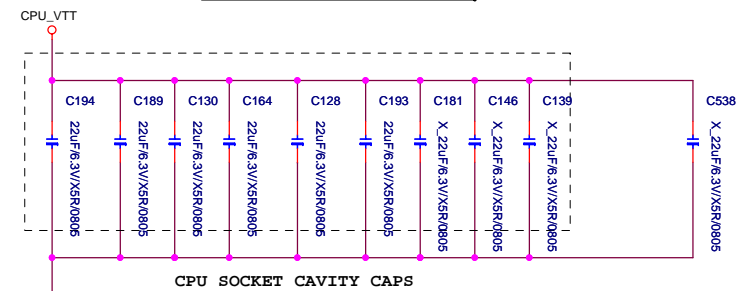
+CPU_VCCP-Decoupling



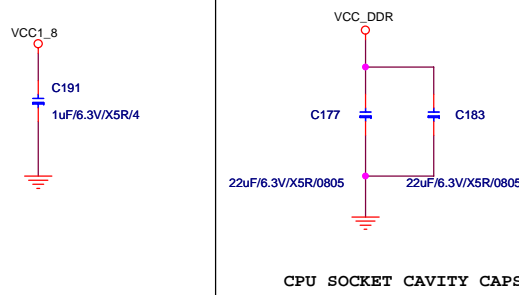
+CPU_GFX Decoupling



+CPU_VTT Decoupling



+1.5V_DDR3-Decoupling



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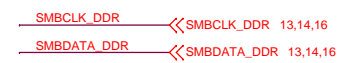
Size Custom	Document Description CPU-Decoupling	Rev 10
Date: Tuesday, July 21, 2009	Sheet 12 of 53	

VCC3 VTT_DDR



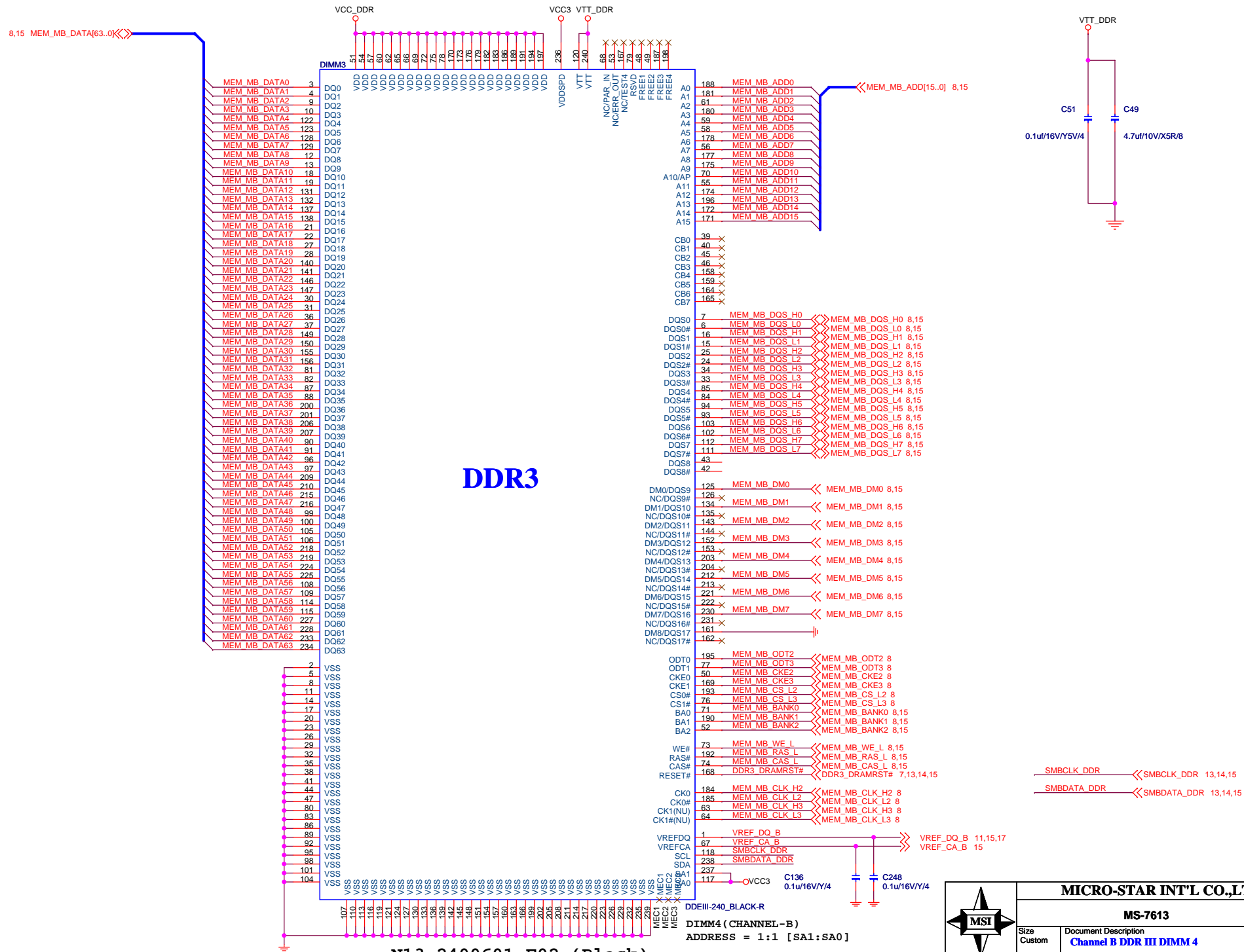
MICRO-STAR INT'L CO.,LTD			
MS-7613			
Size Custom	Document Description Channel A DDR III DIMM 2		Rev 10
Date: Tuesday, July 21, 2009		Sheet 14 of	53

N13-2400921-F02 (Blue)

**MS-7613**

Size Custom	Document Description Channel B DDR III DIMM 3	Rev 10
Date: Tuesday, July 21, 2009		Sheet 15 of 53

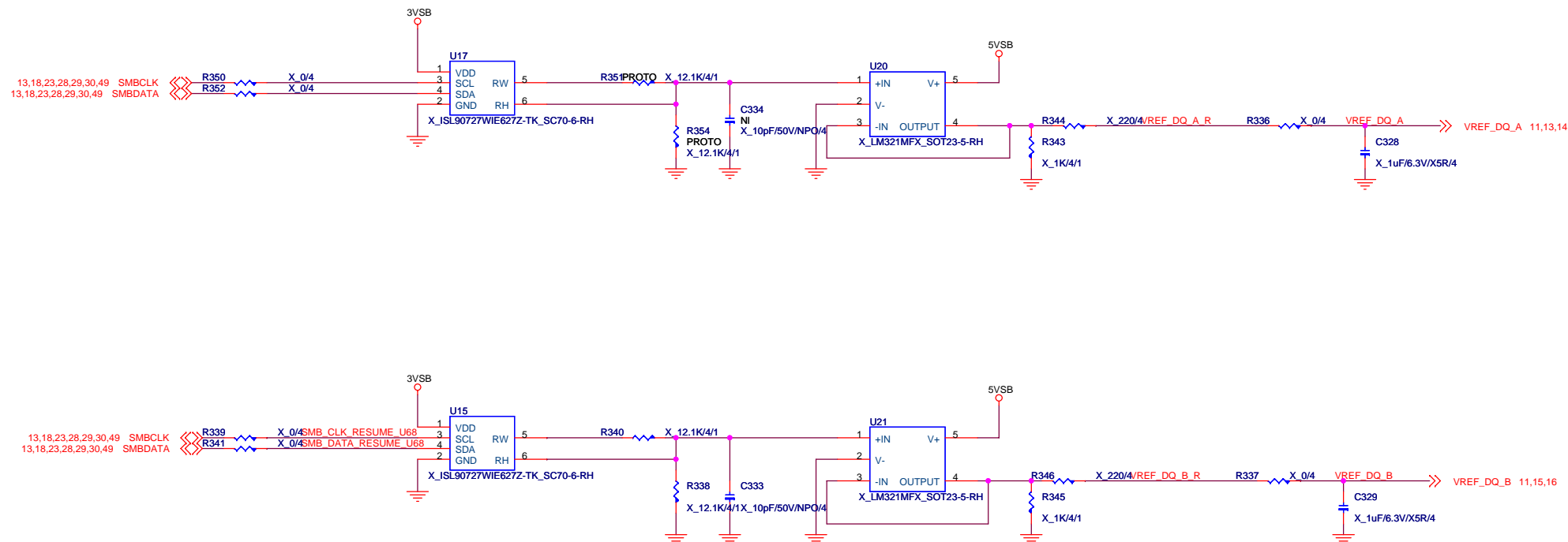
DDRIII DIMM_B2



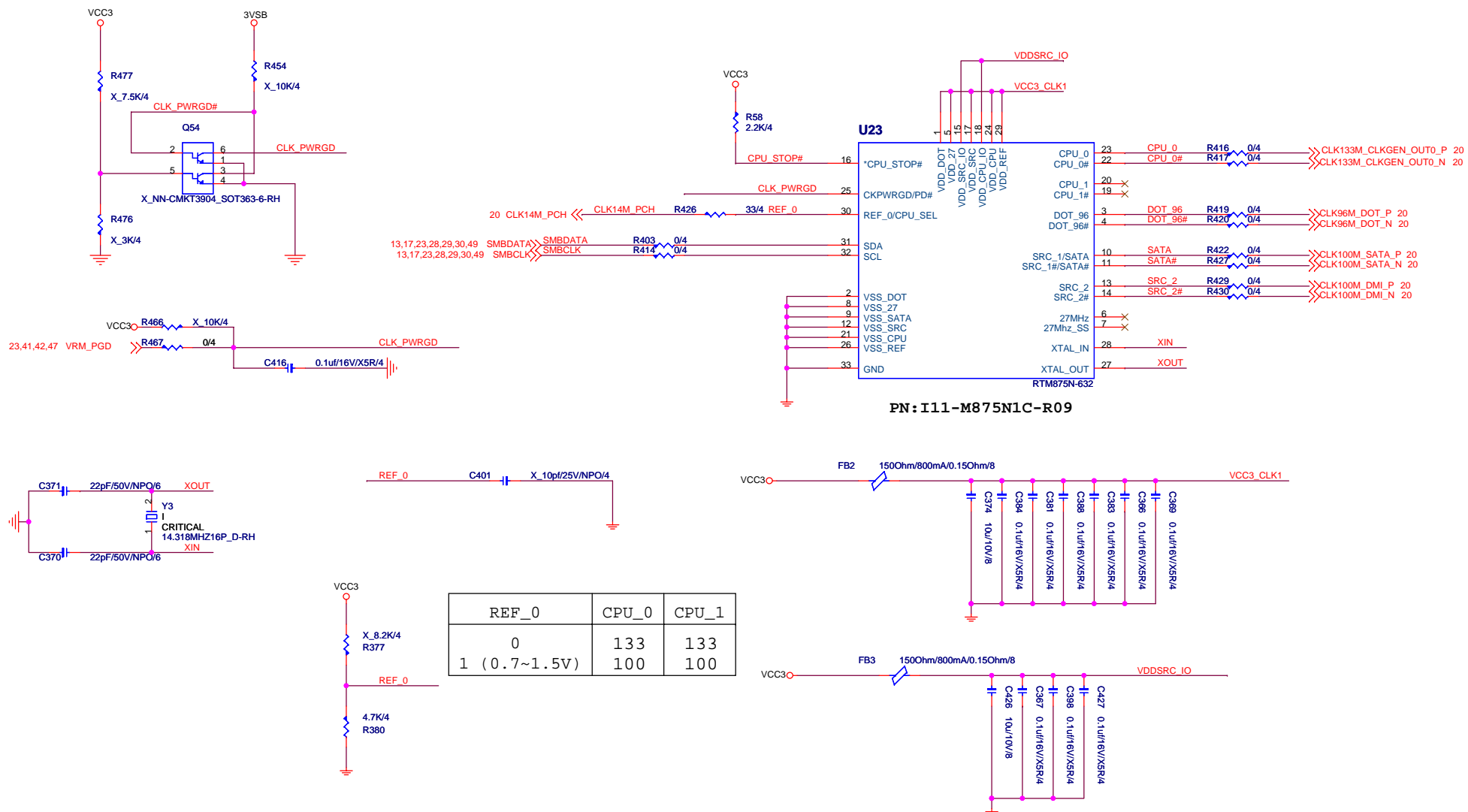
MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description Channel B DDR III DIMM 4	Rev 10
Date: Tuesday, July 21, 2009	Sheet 16 of 53	



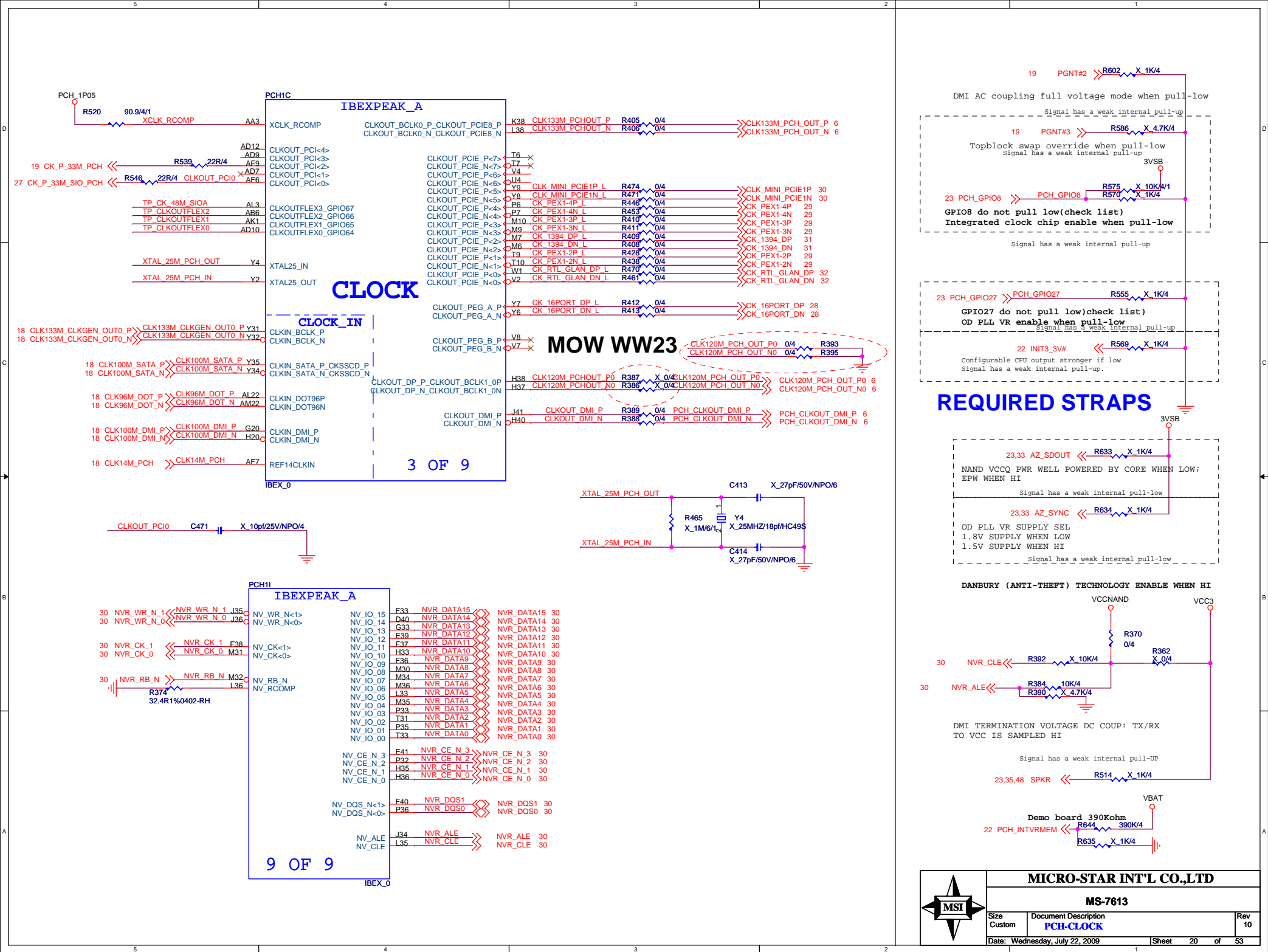
MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size	Document Description	Rev
Custom	DIMM VREF (Option)	10
Date: Tuesday, July 21, 2009		
Sheet	17	of 53

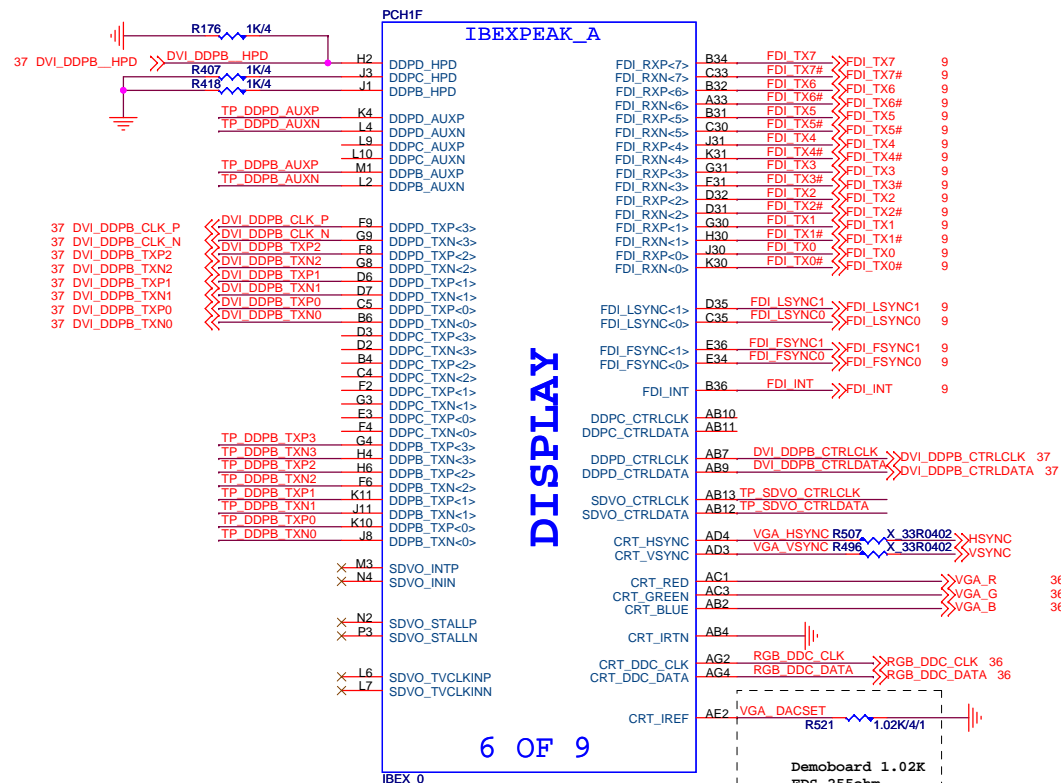


PN: I11-M875N1C-R09

REF_0	CPU_0	CPU_1
0	133	133
1 (0.7~1.5V)	100	100

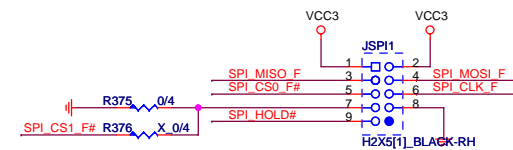






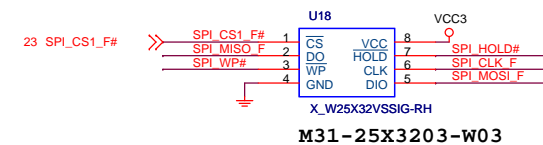
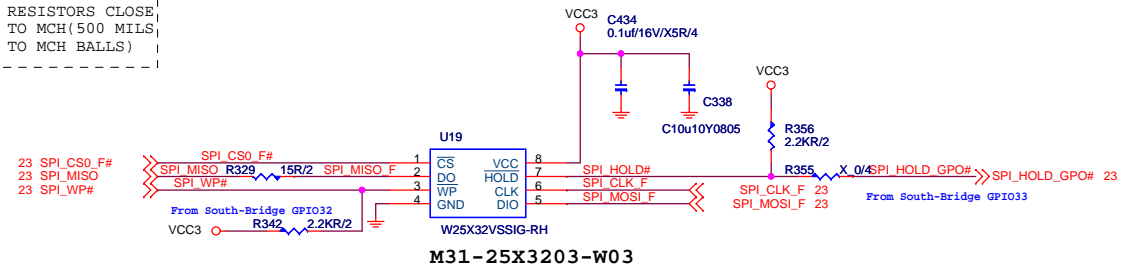
SPI DEBUG PROT

Close to SPI ROM

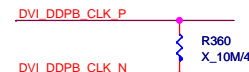


Part Number:N31-2051451-H06

SPI FLASH ROM



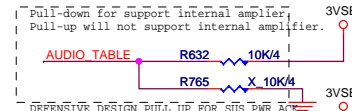
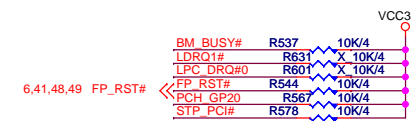
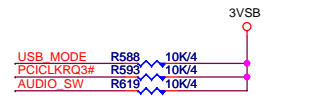
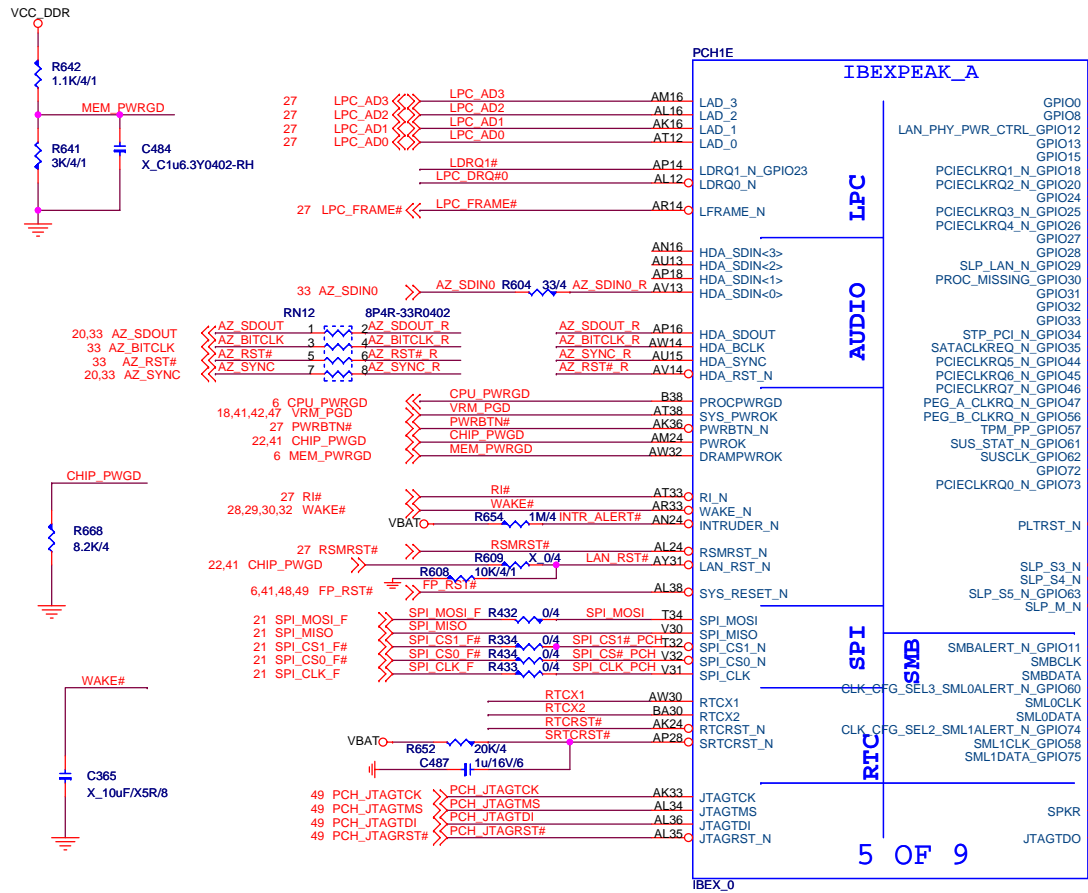
R360 is TEST POINT closer Chipset



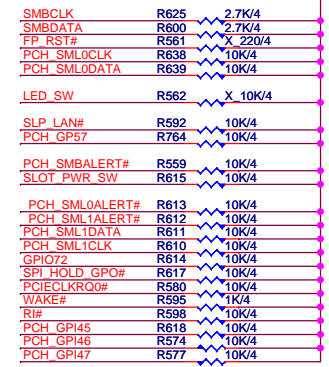
MICRO-STAR INT'L CO.,LTD

MS-7613

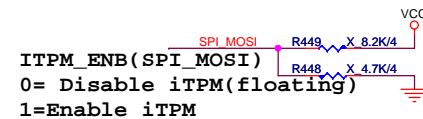
Size	Document Description	Rev
Custom	PCH-DISPLAY/ SPI ROM	10
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GPIO15(SPI_HOLD_GPO#) Demo board 1.0 change to high
TLS CONFIDENTIALITY DISABLE WHEN LOW



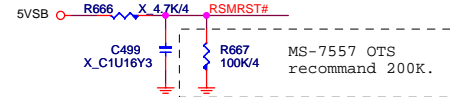
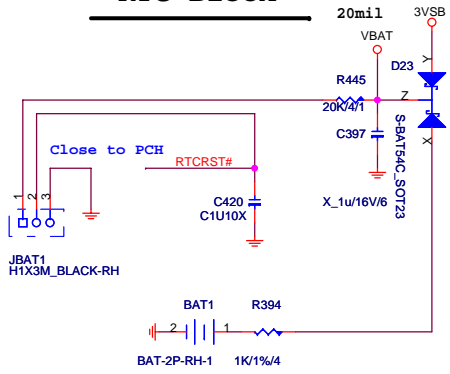
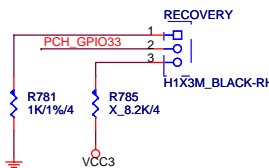
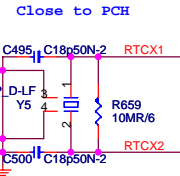
Disable ME in Manufacturing Mode
(GPIO33 Pull Down 1K)



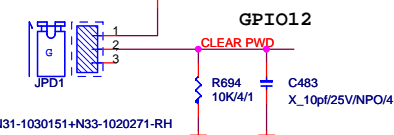
CMOS CLEAR JUMPER	
1 - 2	Normal
2 - 3	Clear CMOS

RTC Block

RECOVERY JUMPER	
1 - 2	ENABLE
2 - 3	DISABLE



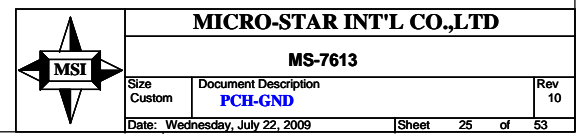
Password CLEAR JUMPER	
1 - 2	Normal
2 - 3	Clear PD



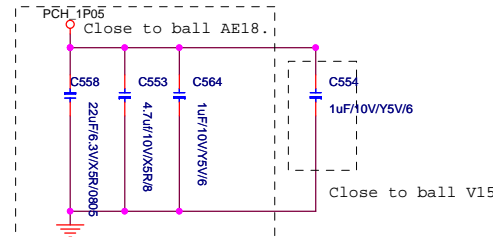
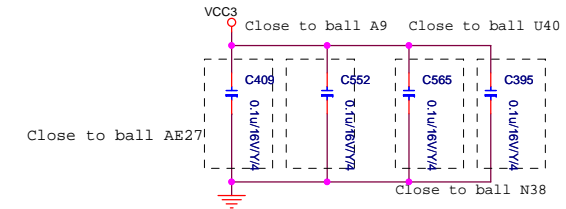
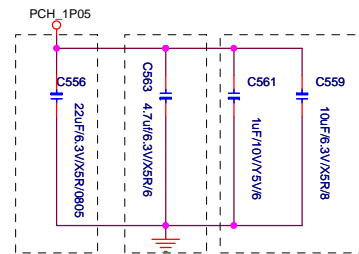
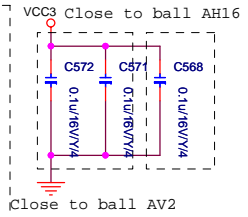
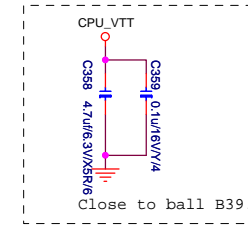
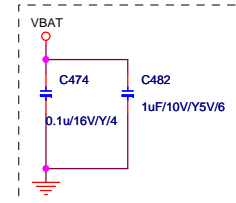
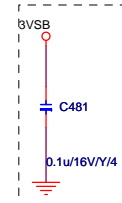
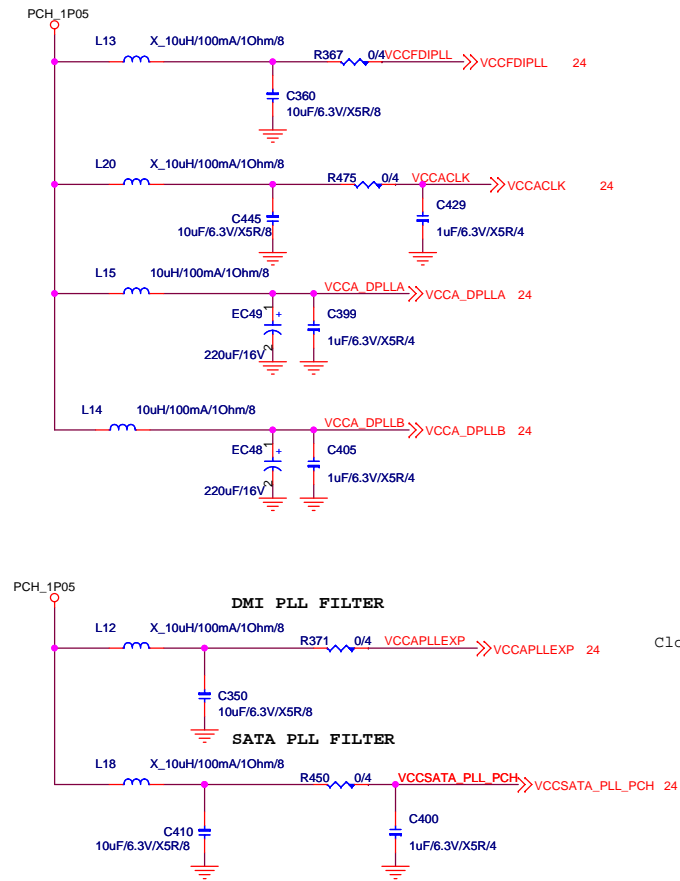
MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	PCH-SMB/LPC/AUDIO/RTC	10
Date: Wednesday, July 22, 2009	Sheet 23 of 53	

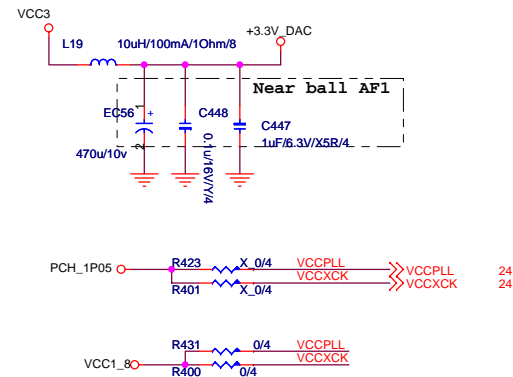
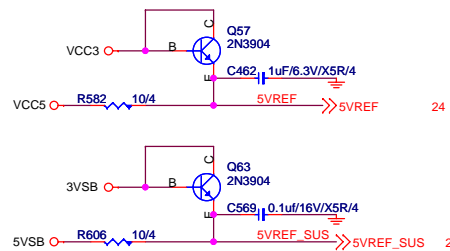


PCH decoupling cap



5VREF & 5VREF_SUS Sequencing Circuit

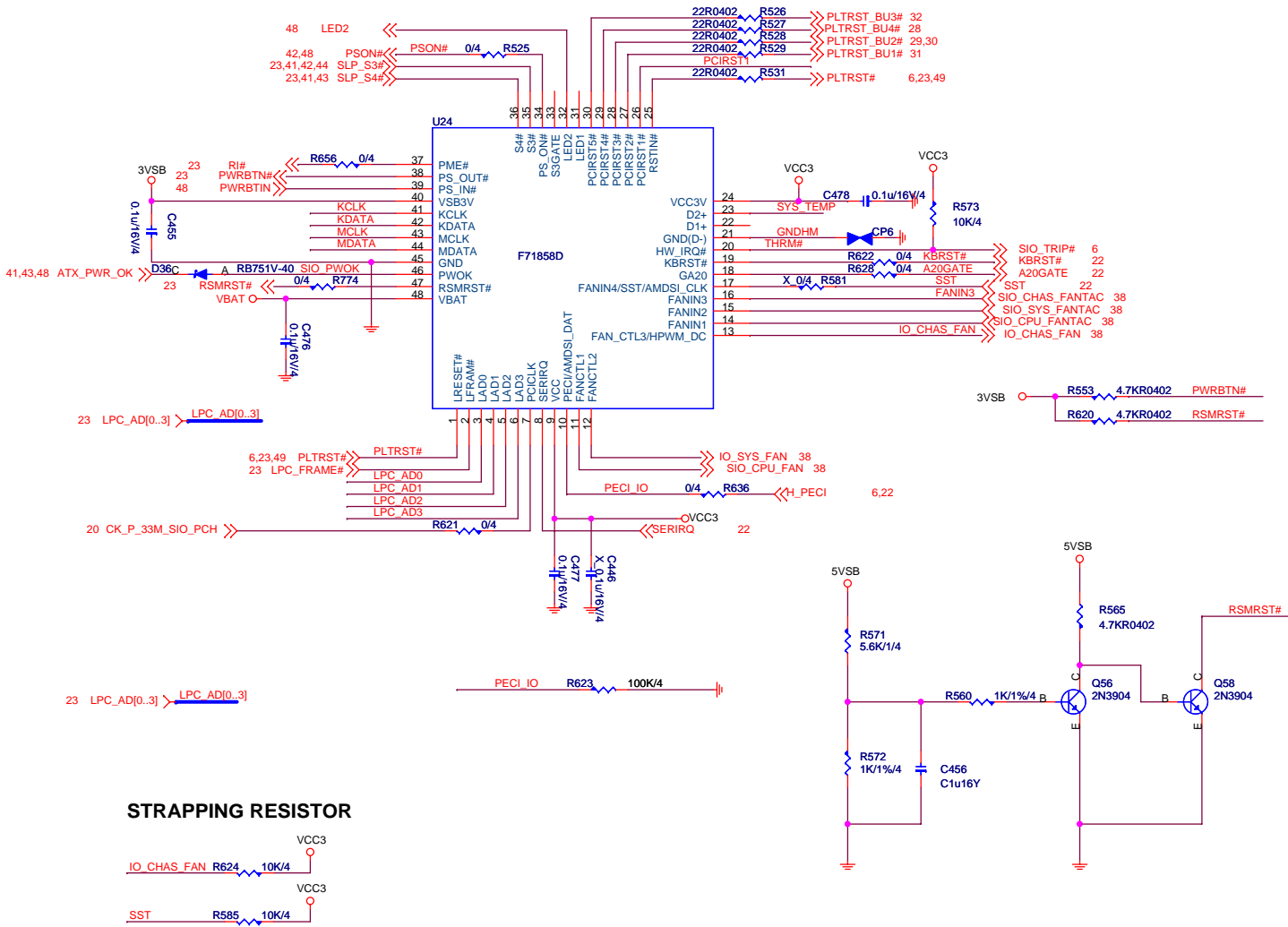
5VREF must be powered up before VCC3 or after VCC3 within 0.7V.
Also, 5VREF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to 5VREF_SUS and 3VSB.
However, the 3VSB is derived from the 5VSB on the power supply
thru a voltage regulator and therefore, they can satisfy the requirement.



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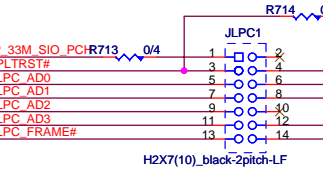
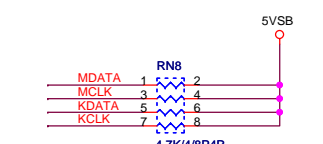
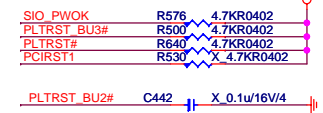
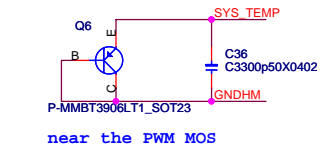
Size	Document Description	Rev
Custom	PCH-DECOUPLING	10
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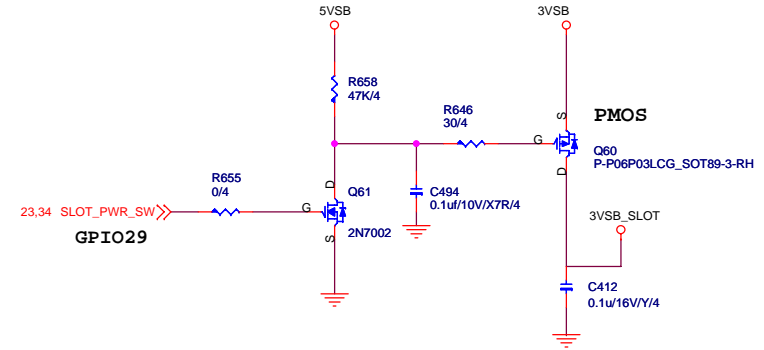
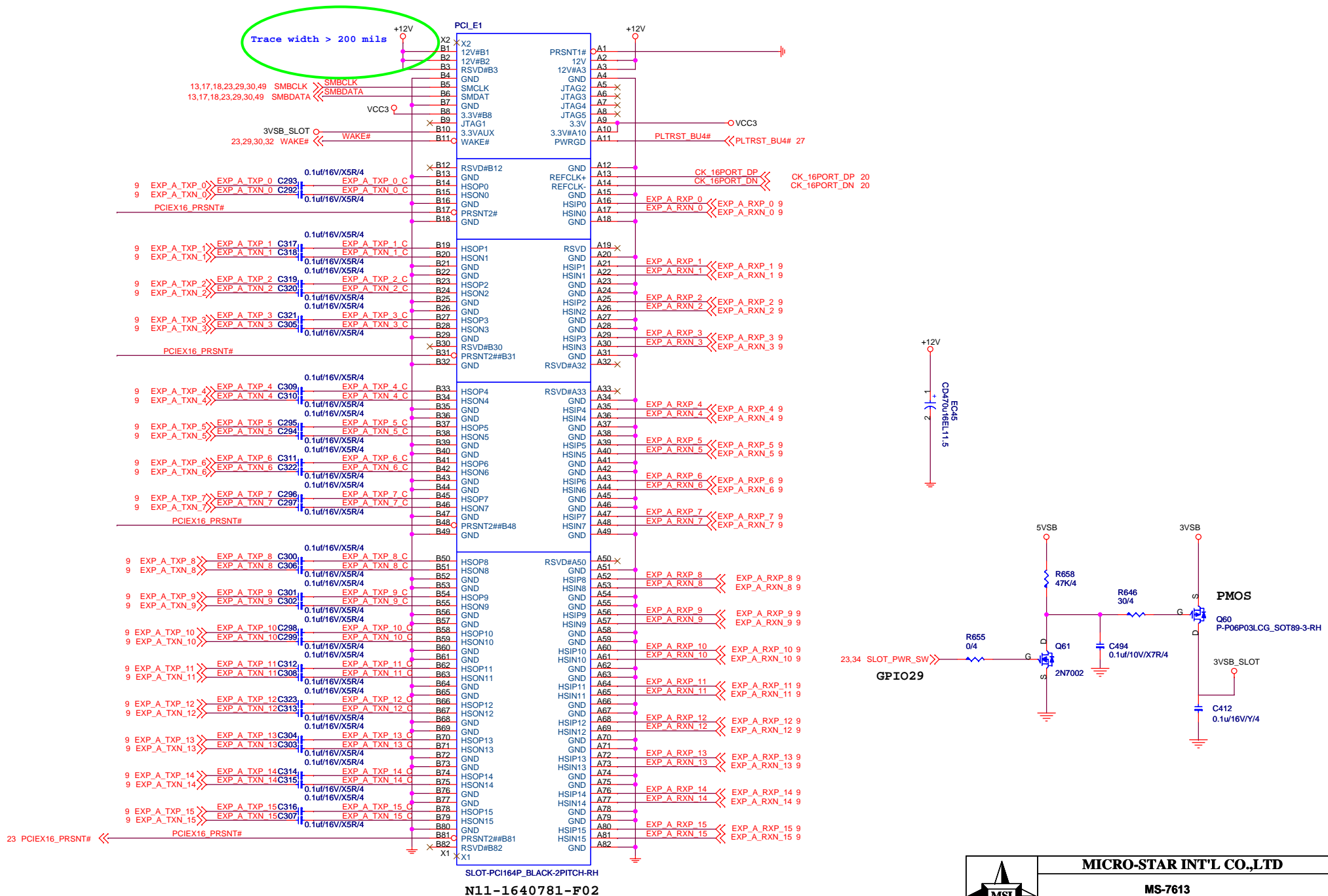
STRAPPING RESISTOR

Pin	Function	Net name	HI	NC
13	FWH_TRAP	IO_CHAS_FAN	Fan control method will be PWM Mode	Fan control method will be DAC Mode

SYSTEM TEMP



PCI_Express X16 Slot

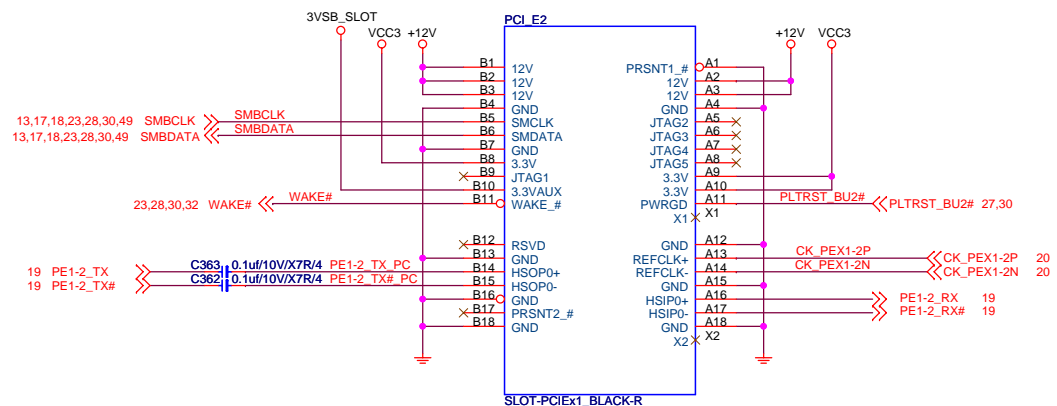


MICRO-STAR INT'L CO.,LTD

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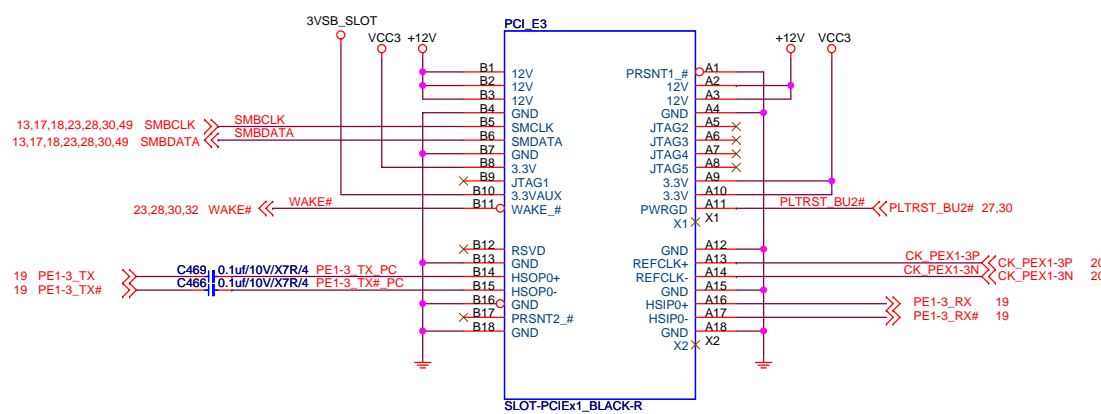
Size Custom	Document Description PCIE X16 SLOT	Rev 10
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PCI EXPRESS x1-PORT1



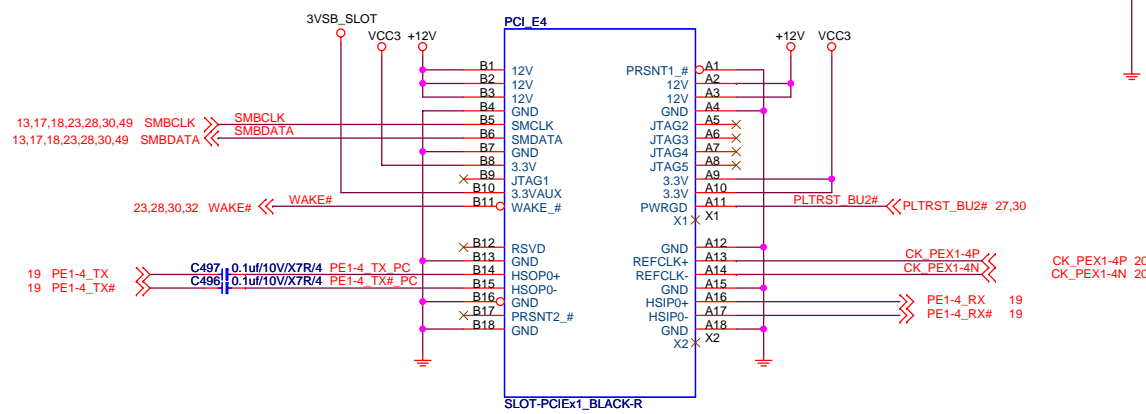
N11-0360281-K06

PCI EXPRESS x1-PORT2

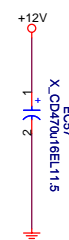


N11-0360281-K06

PCI EXPRESS x1-PORT3



N11-0360281-K06



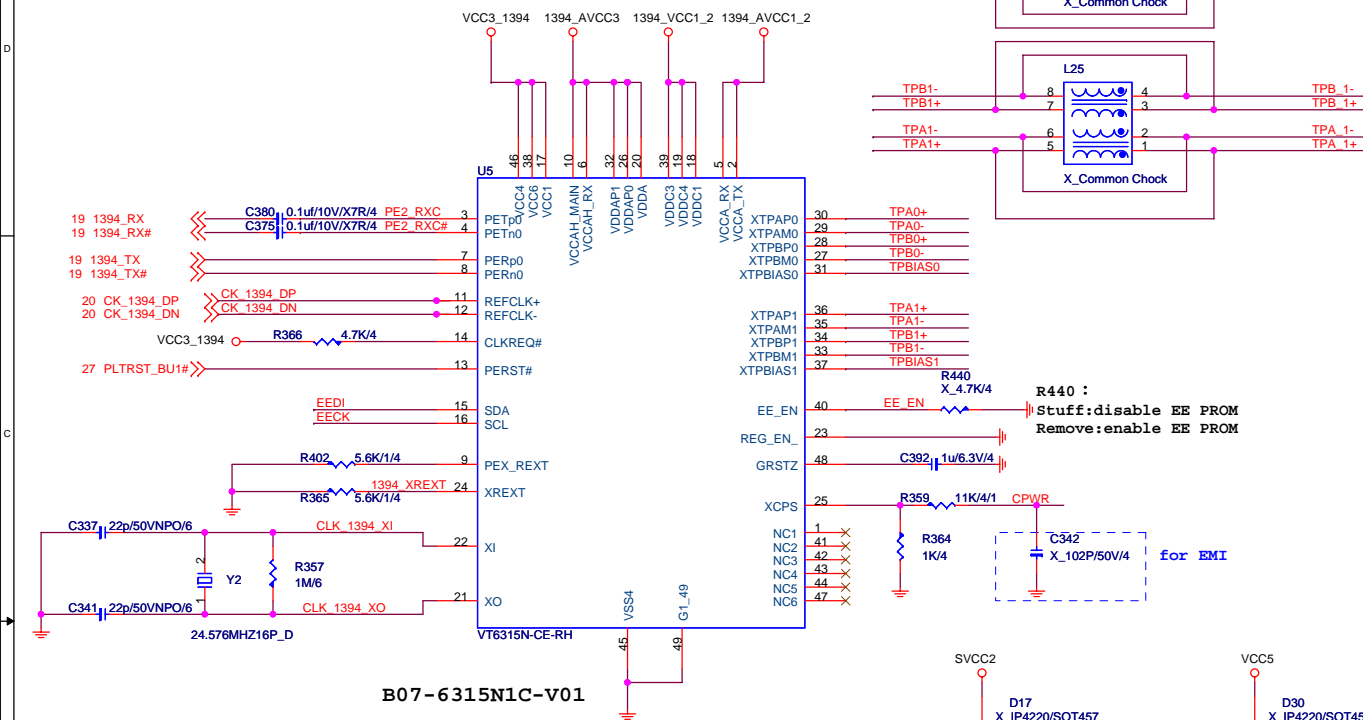
MICRO-STAR INT'L CO.,LTD

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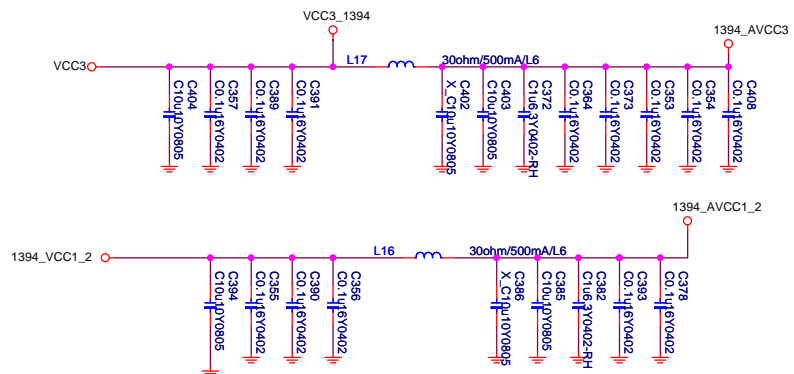
Size	Document Description	Rev
Custom	PCIE X1 SLOT	10

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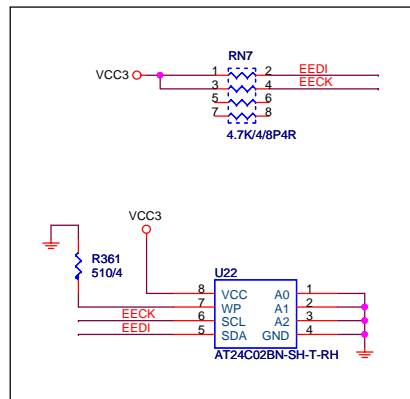
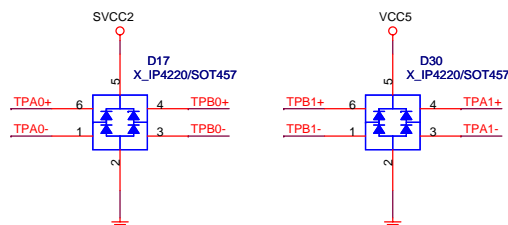
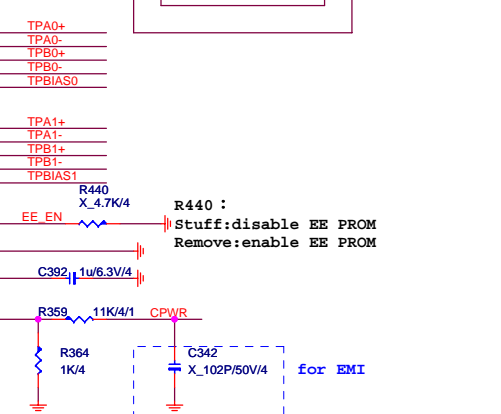
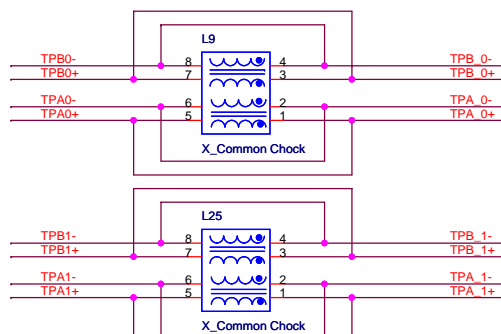
1394 CONTROLLER



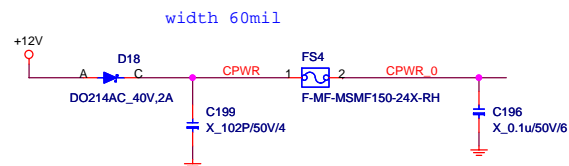
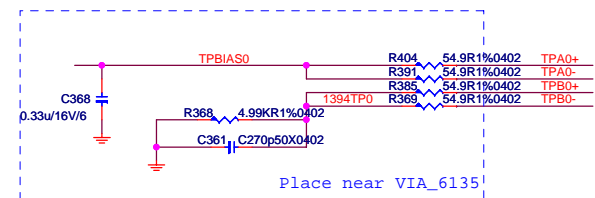
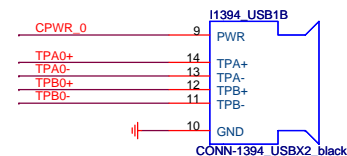
close to chip of all Cap.



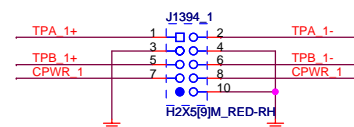
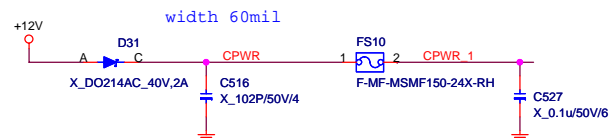
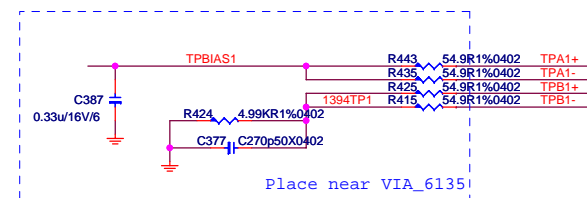
close to chip of all Cap.



Rear 1394 port



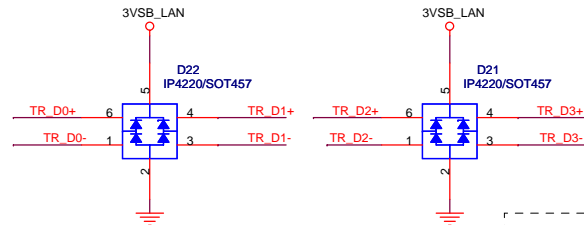
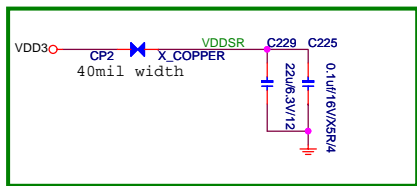
Front 1394 pin header



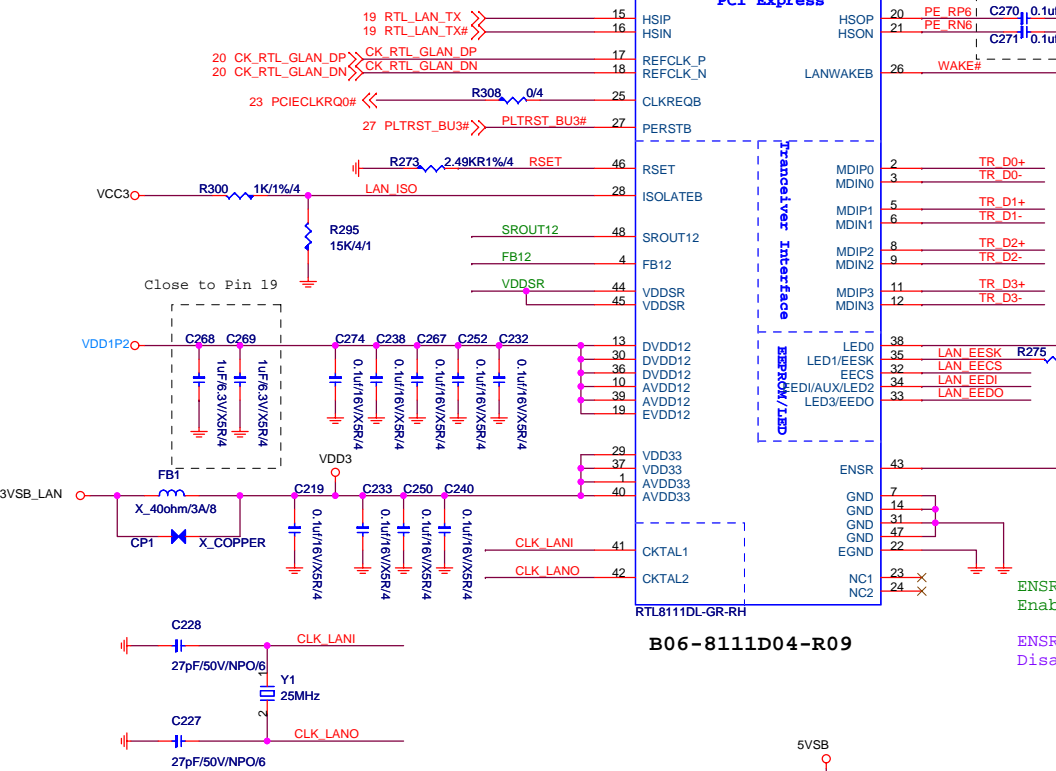
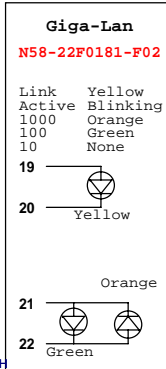
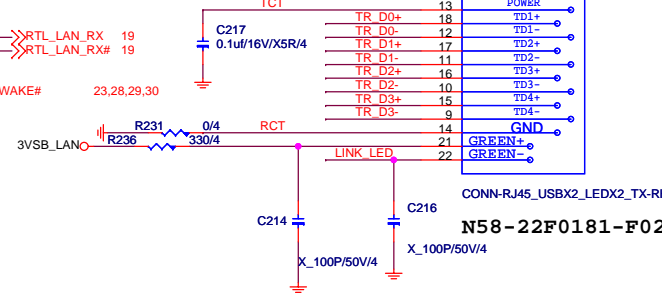
For Intel 1394 pinheader



MICRO-STAR INT'L CO.,LTD			
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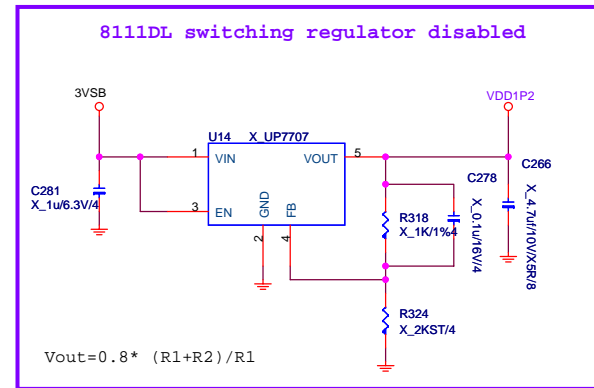


Closed 8111DL

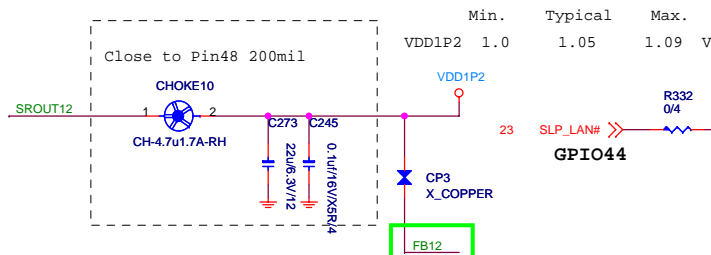


ENSR=1,
Enable switching regulator

ENSR=0,
Disable switching regulator

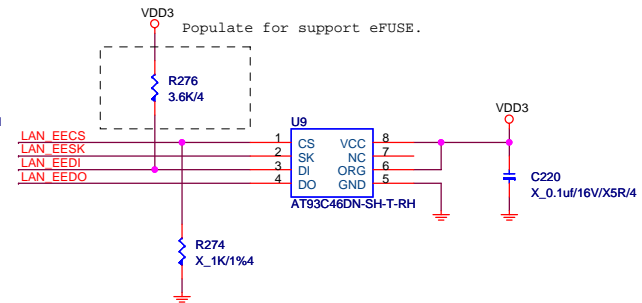
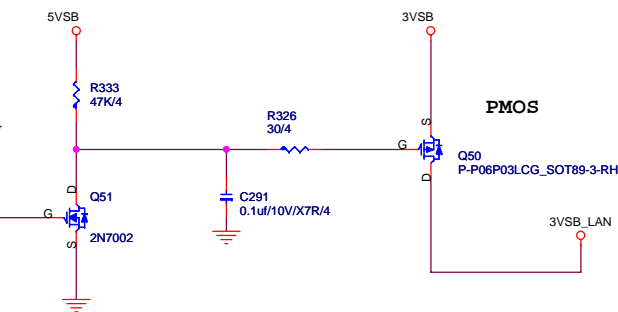


$$V_{out} = 0.8 * (R1 + R2) / R1$$



	Min.	Typical	Max.
VDD1P2	1.0	1.05	1.09 V

GPI044



"FB12": A trace from CHOKE to RTL8111DL pin4



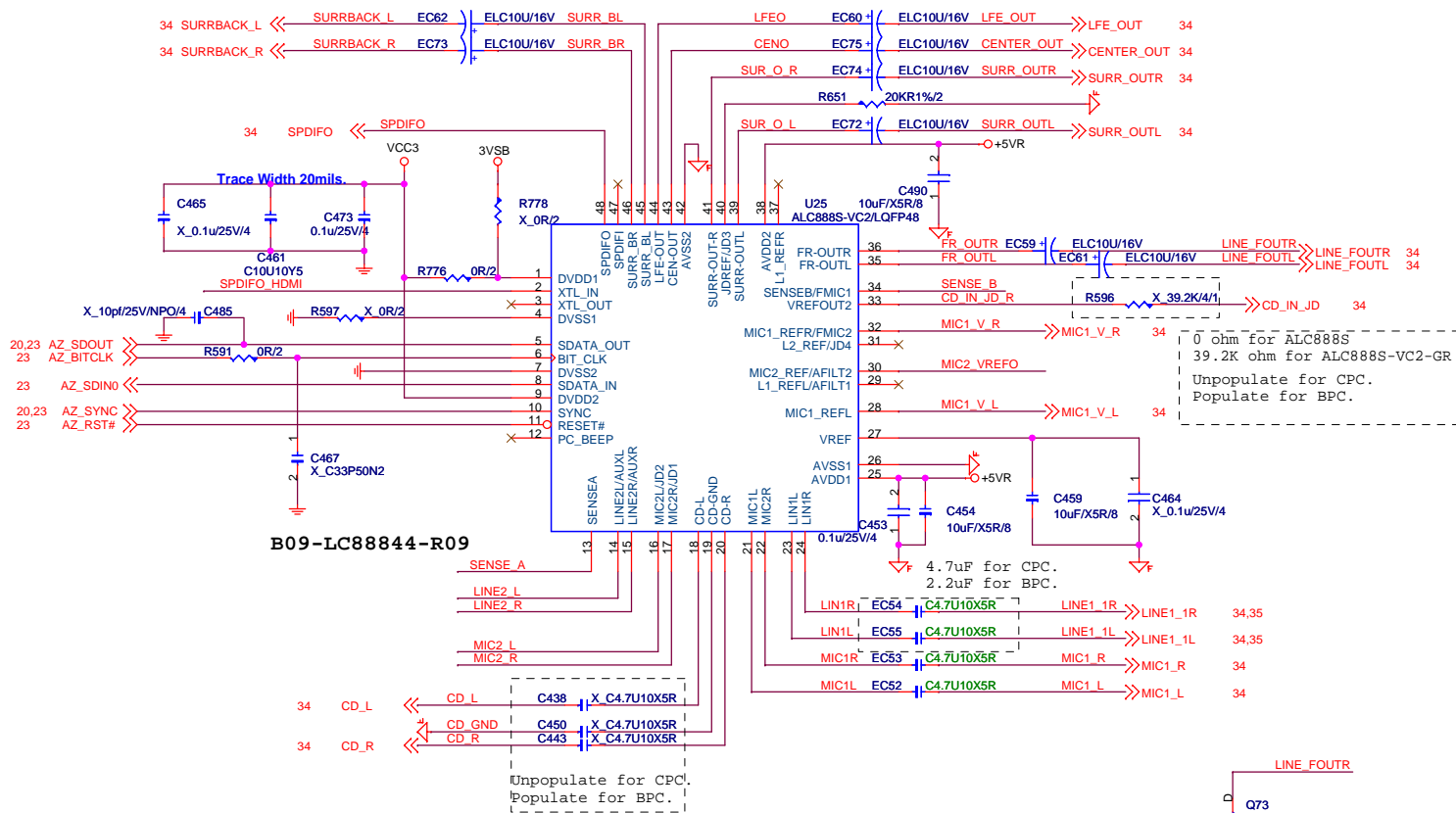
MICRO-STAR INT'L CO.,LTD

MS-7613

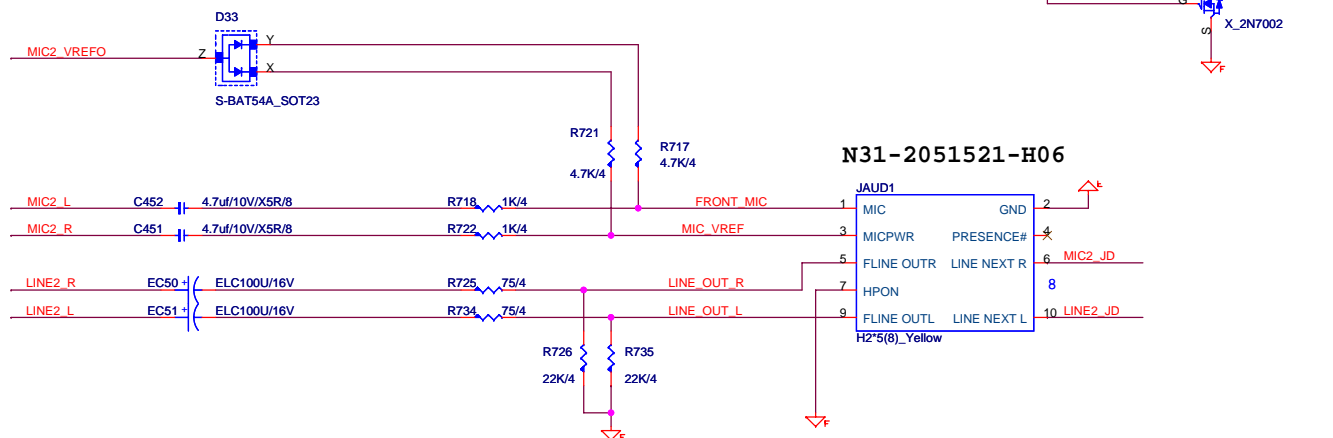
Size	Document Description	Rev
Custom	LAN-RTL8111DL	10

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ALC888S CODEC

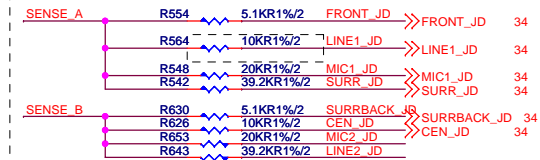


Azalia Front Audio Connector



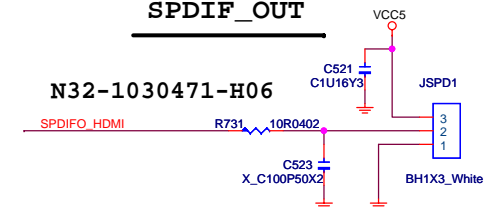
ALC888S JACK DETECT

```
Populate R564 for CPC.
Unpopulate R564 for BPC.
```

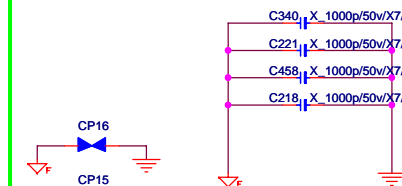


SPDIF_OUT

N32-1030471-H06



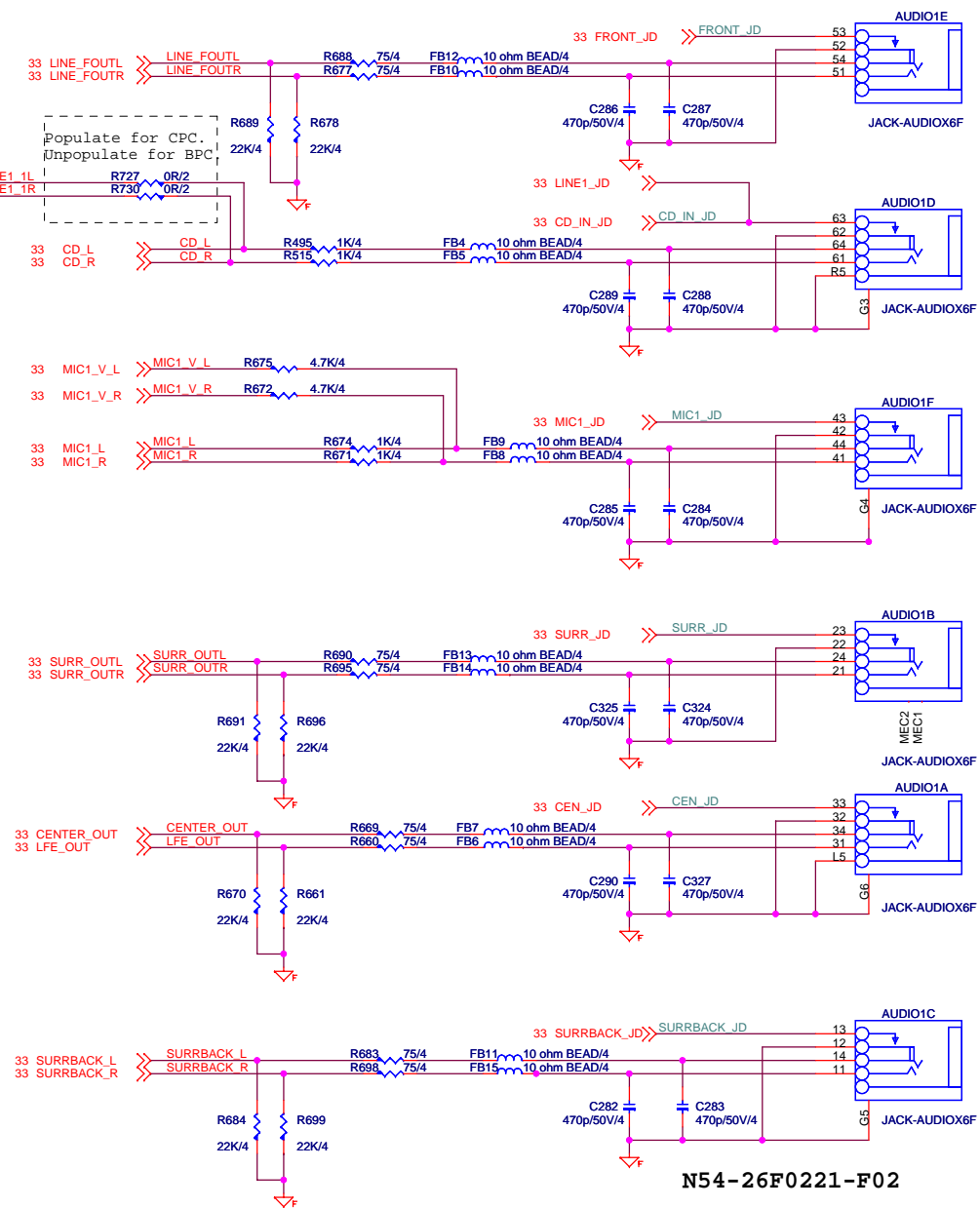
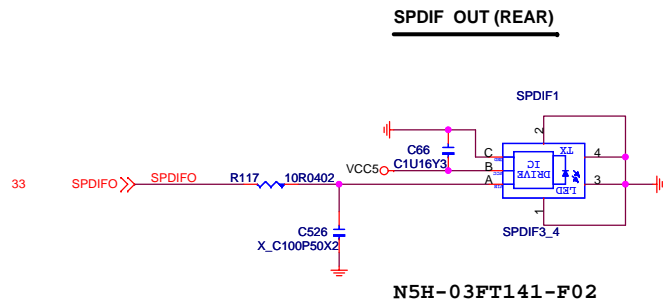
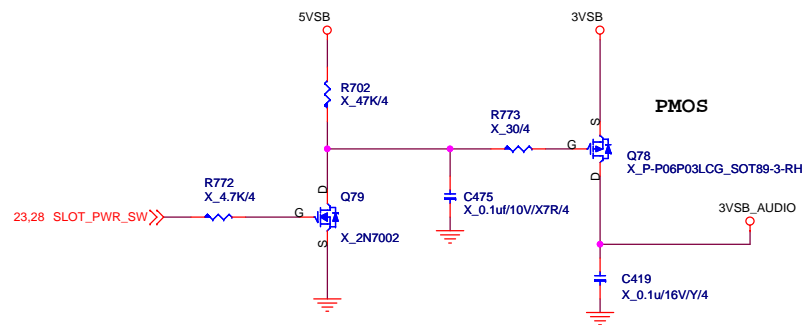
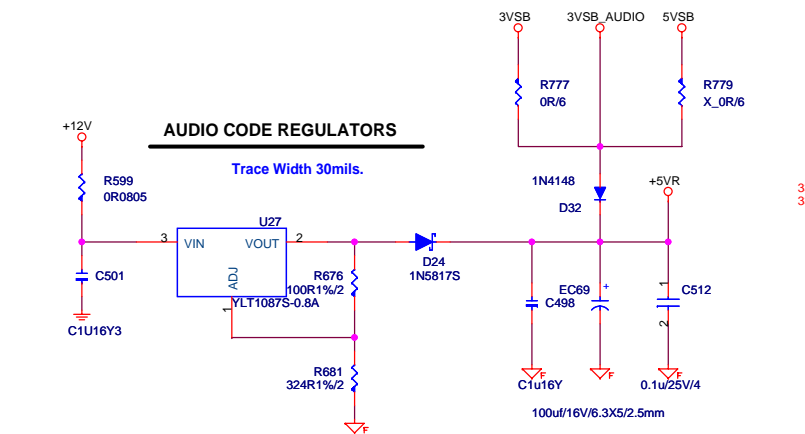
For EMI



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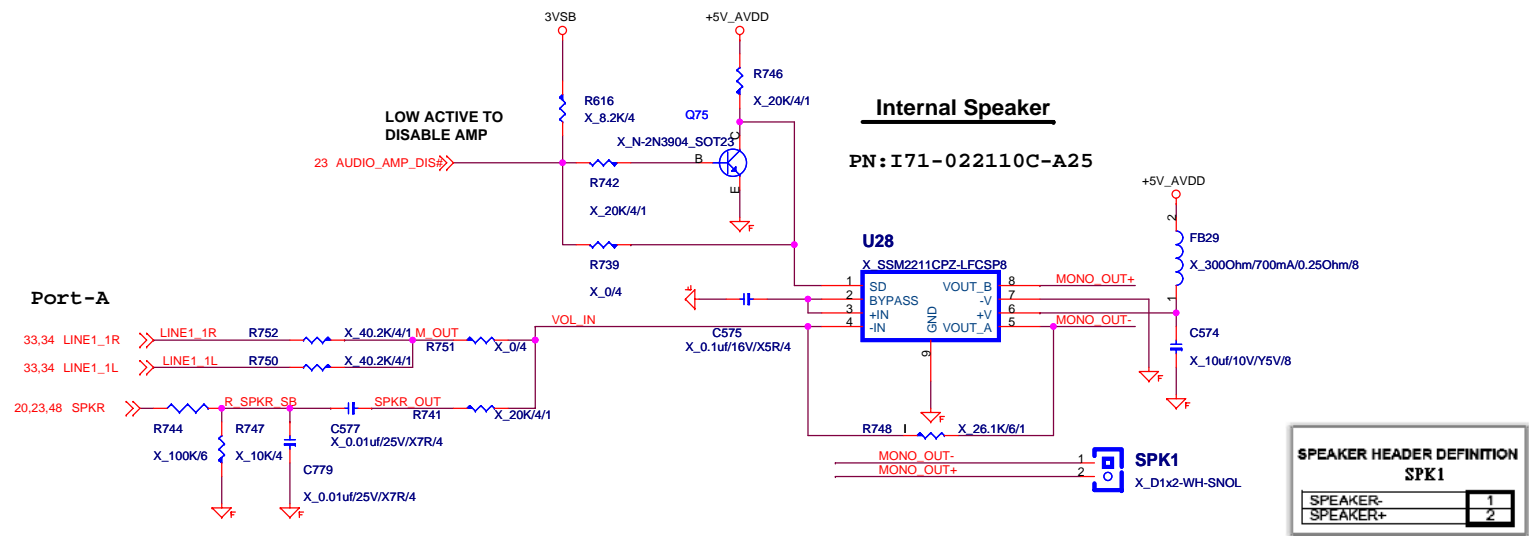
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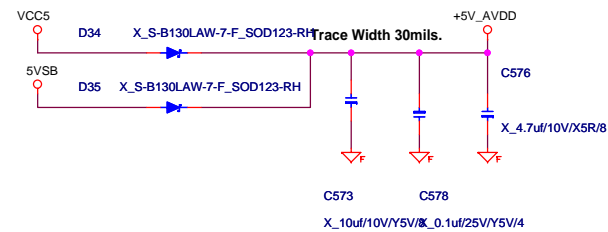
MICRO-STAR INT'L CO.,LTD

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Custom	AUDIO JACK	10
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AUDIO AMPLIFIER POWER REGULATORS

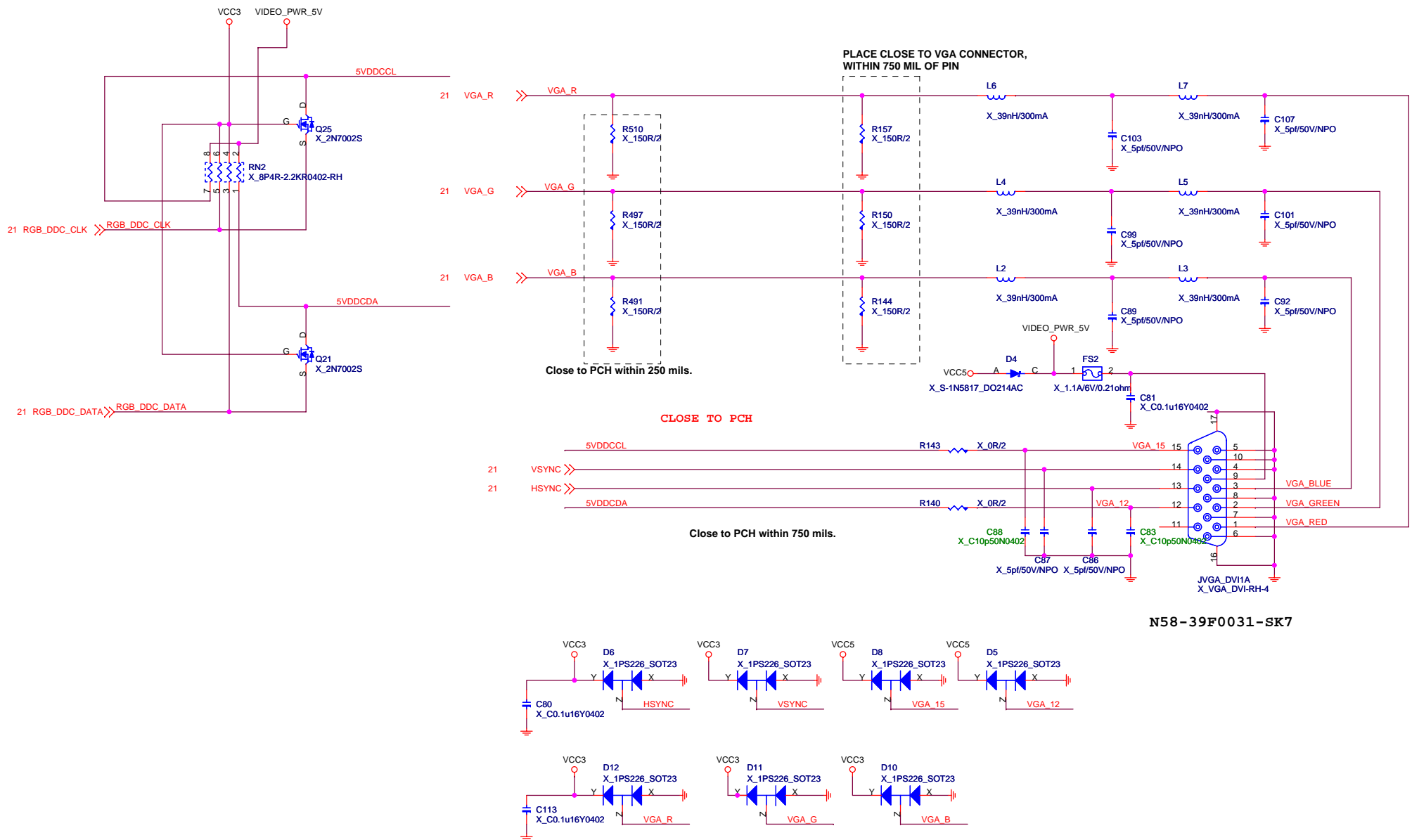


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Custom	AUDIO AMPLIFIER	10
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Video Connector

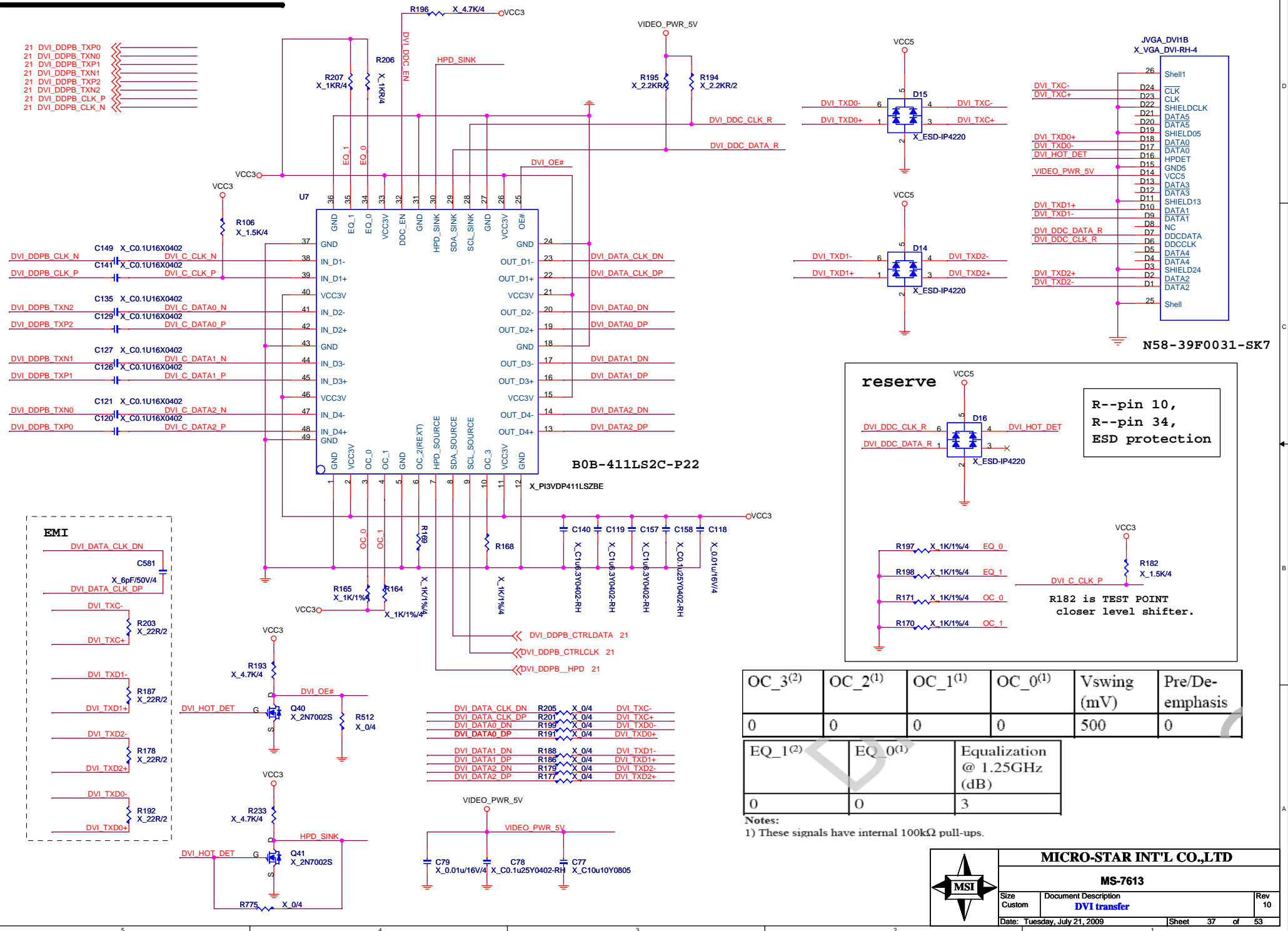


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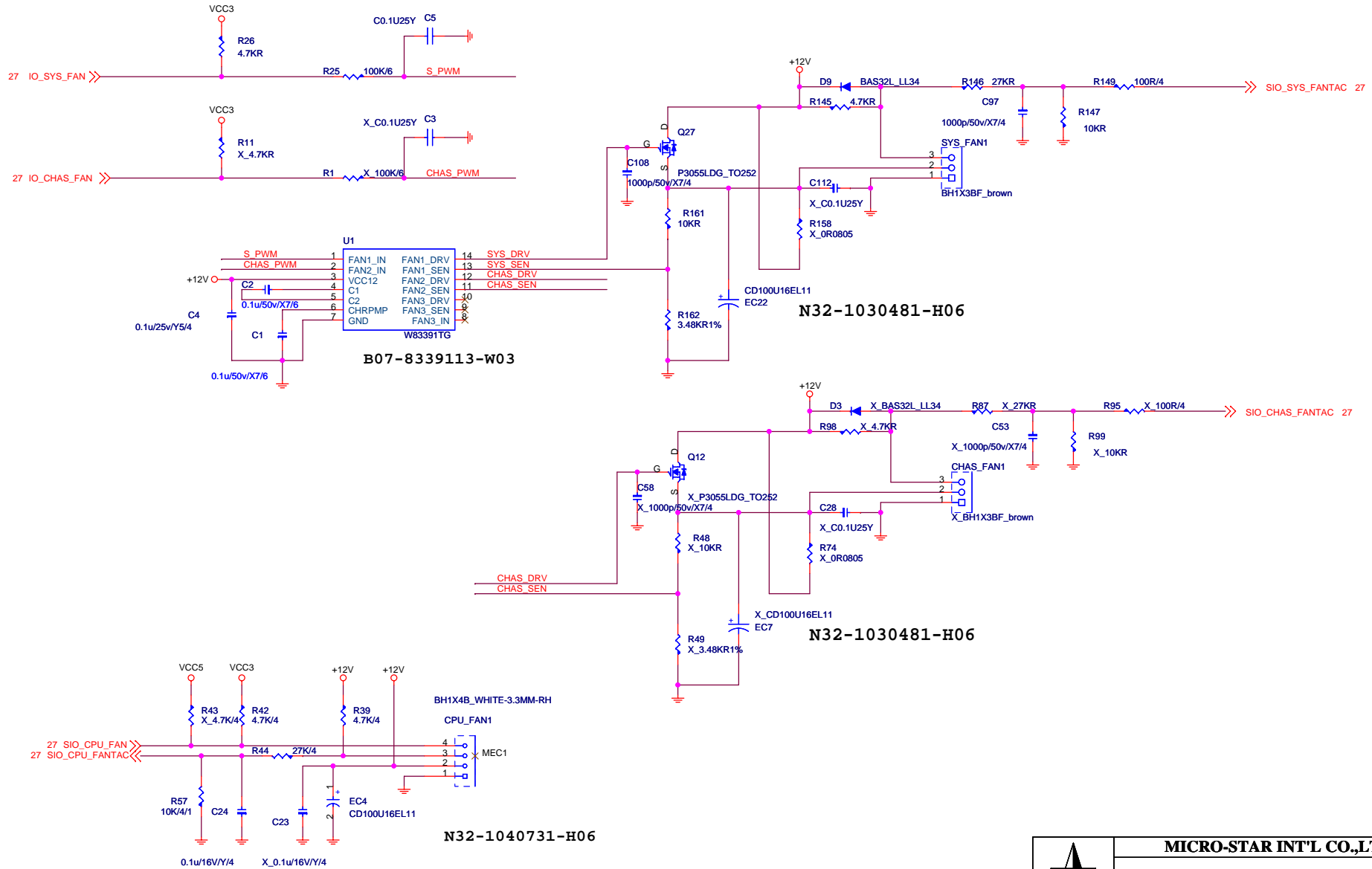
MS-7613

Size	Document Description	Rev
Custom	VGA	10
Date:	Tuesday, July 21, 2009	Sheet 36 of 53

DVI level shifter

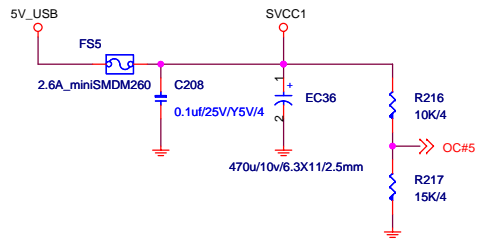


FAN-COUNTROL CIRCUIT

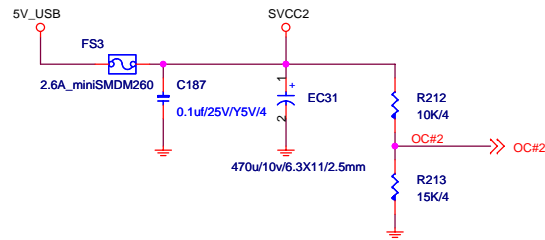


MICRO-STAR INT'L CO.,LTD		
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Size	Document Description	Rev
Custom	FAN Control	10
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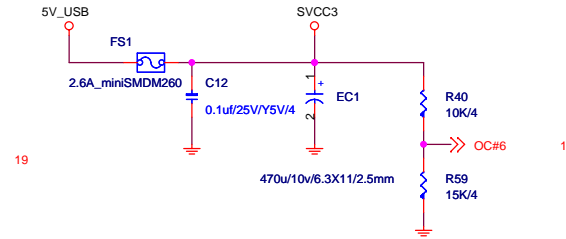
POWER CIRCUIT FOR USB PORT 10, 11



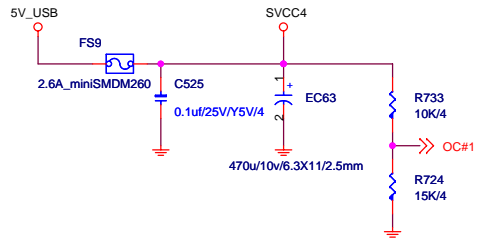
POWER CIRCUIT FOR USB PORT 4, 5



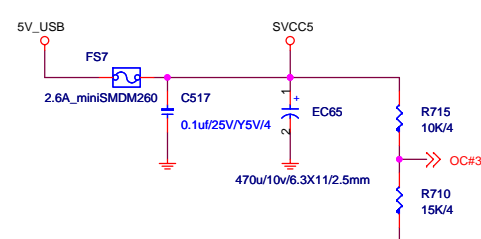
POWER CIRCUIT FOR USB PORT 12, 13



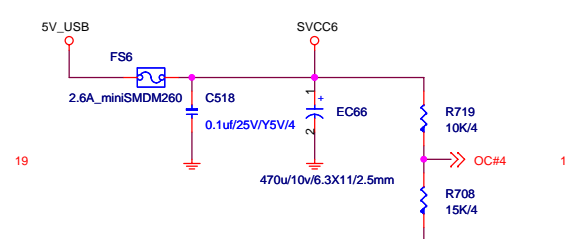
POWER CIRCUIT FOR USB PORT 2, 3



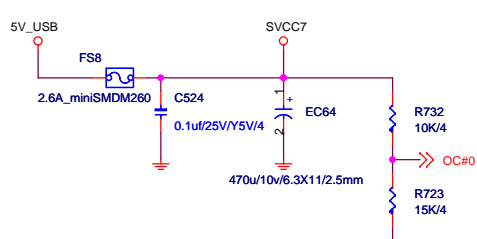
POWER CIRCUIT FOR USB PORT 6, 7



POWER CIRCUIT FOR USB PORT 8, 9



POWER CIRCUIT FOR USB PORT 0, 1



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Size Custom	Document Description USB POWER	Rev 10
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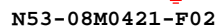
Trace lengths must be less 12 inches



Trace lengths must be less 12 inches



Trace lengths must be less 5 inches



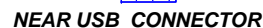
Trace lengths must be less 5 inches



Trace lengths must be less 5 inches



Trace lengths must be less 5 inches



Trace lengths must be less 5 inches



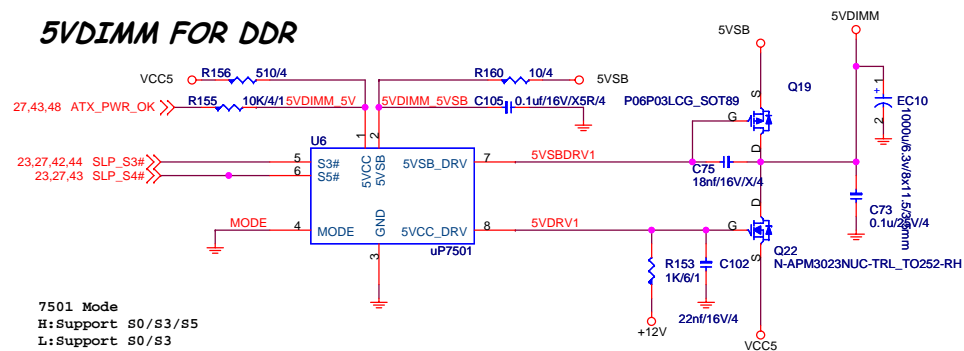
MS-7613

Size	Document Description
Custom	USB Conn.

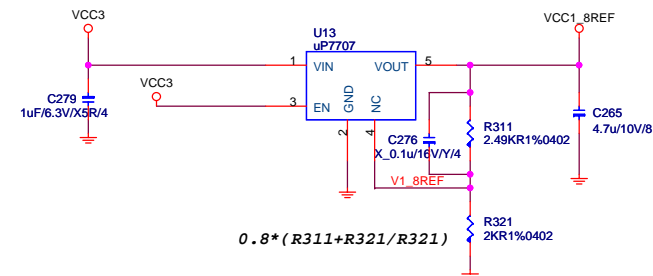
Rev	10
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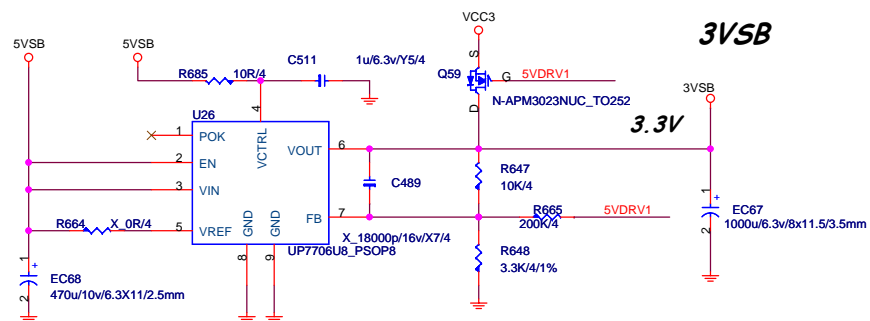
5VDIMM FOR DDR



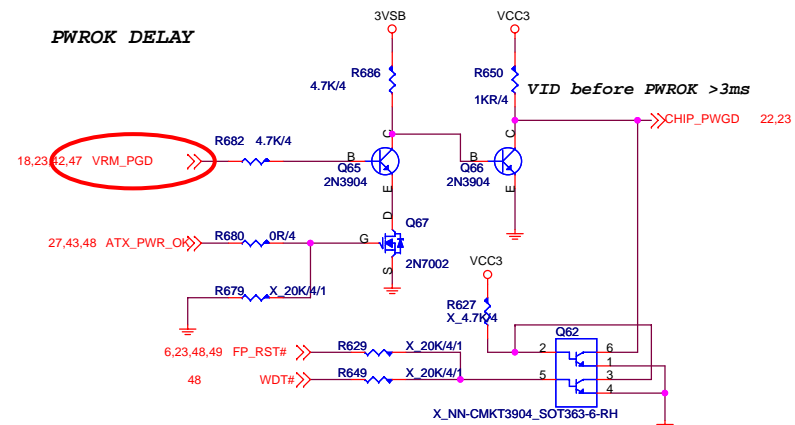
VCC1_8REF



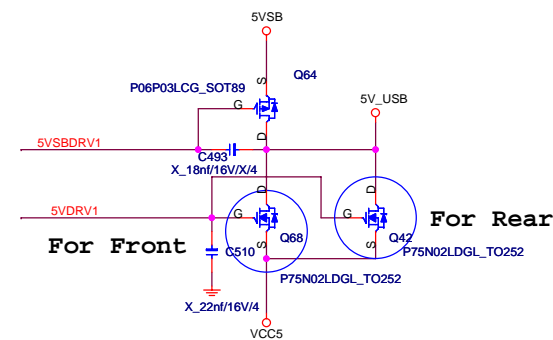
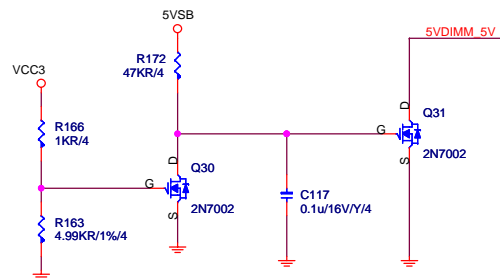
3VSB



PWROK DELAY



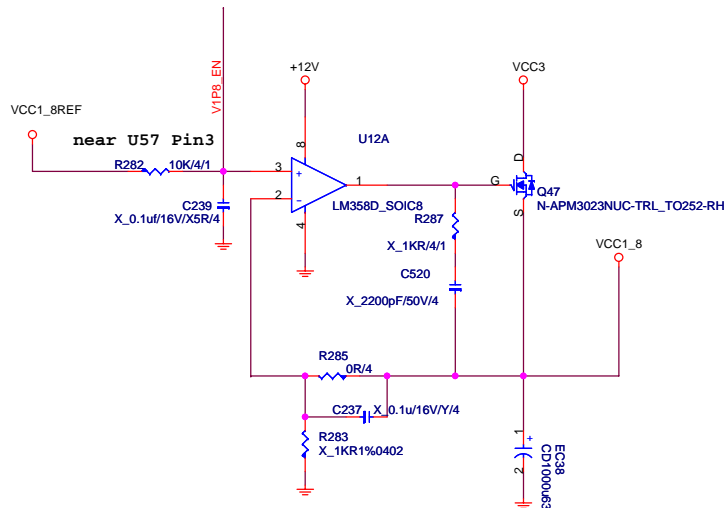
Update from SLP_S3# to VRM_PGD



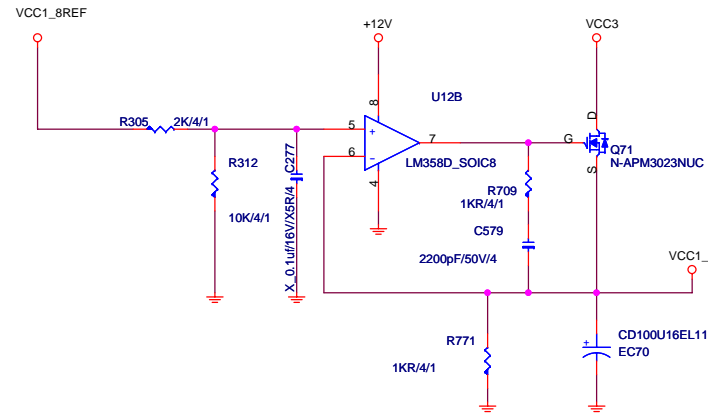
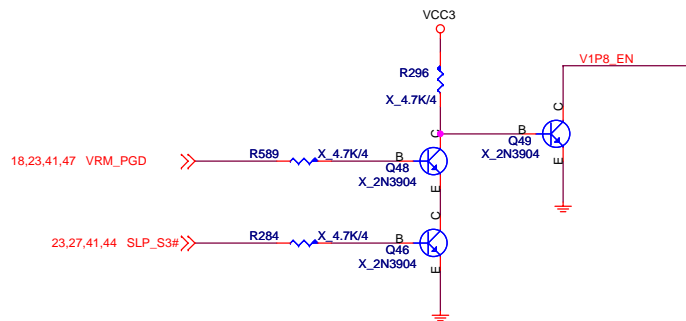
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MS-7613

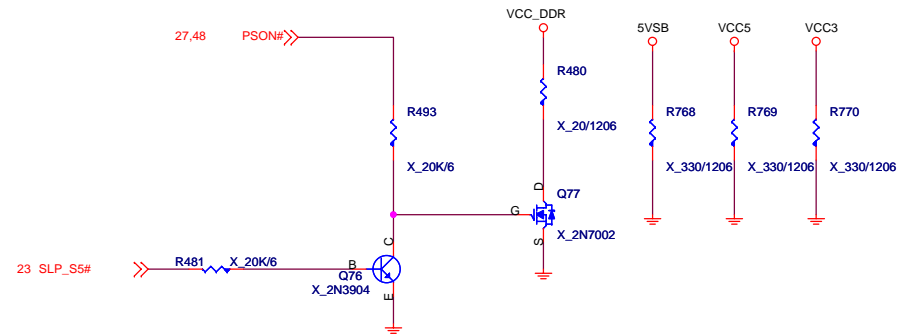
Size Custom	Document Description ACPI Controller 1	Rev 10
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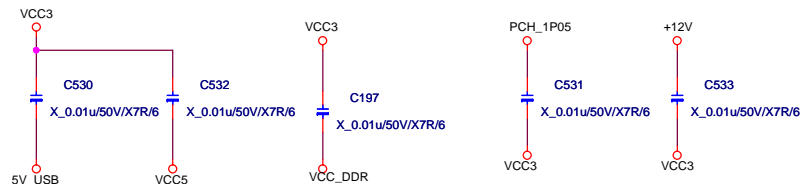
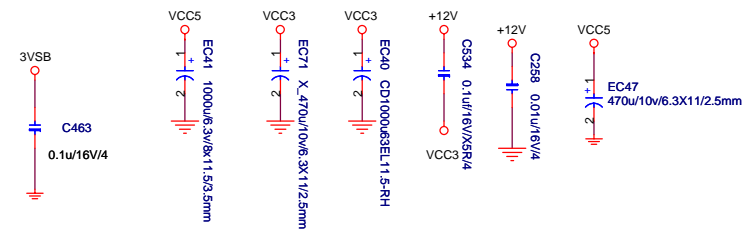
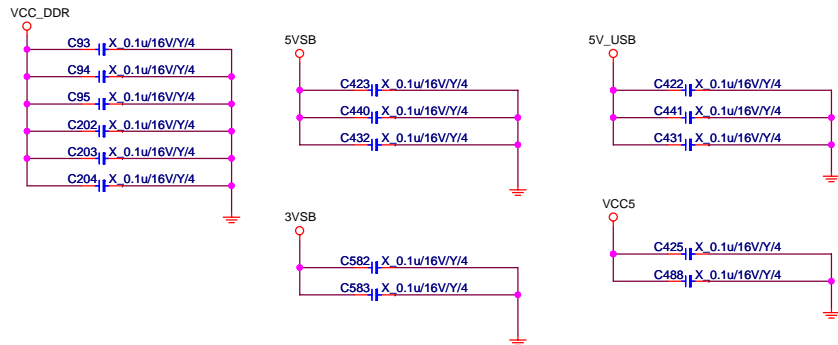
cpuvtt & pch vore wait 1.8v



Discharge Circuit



For EMI



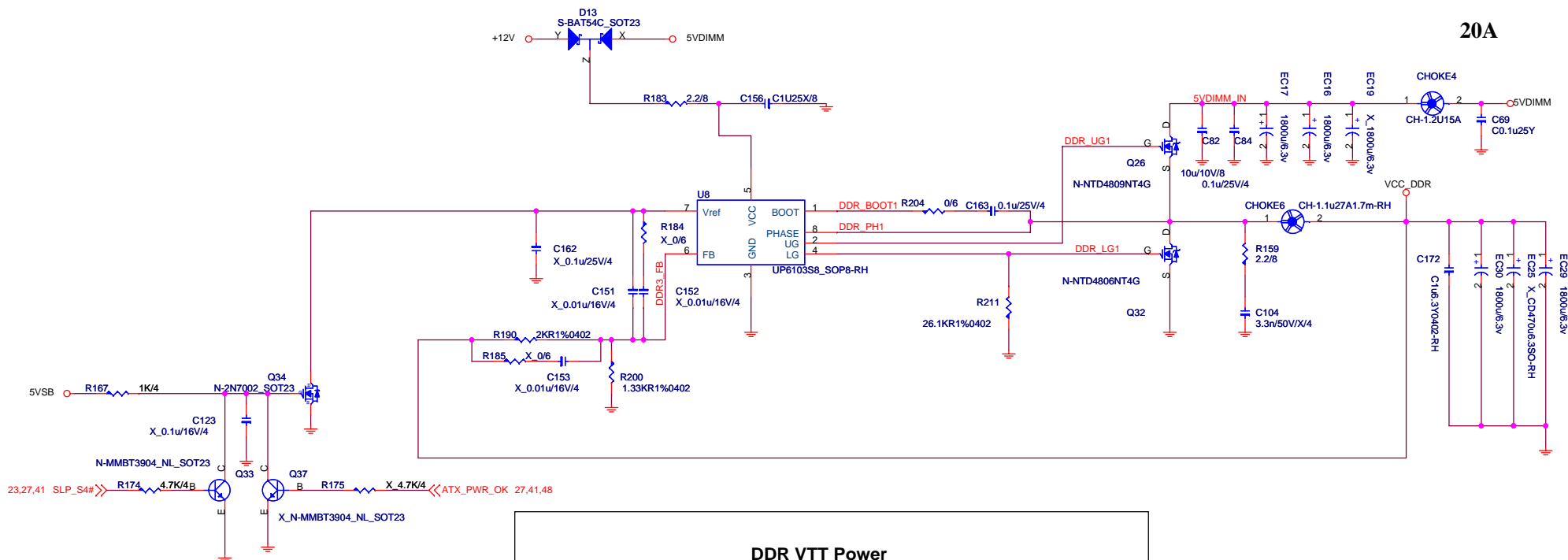
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Size	Document Description	Rev
Custom	ACPI Controller 2	10
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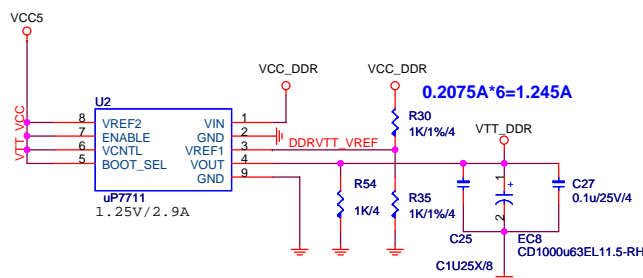
DDR3_1.5V

20A



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



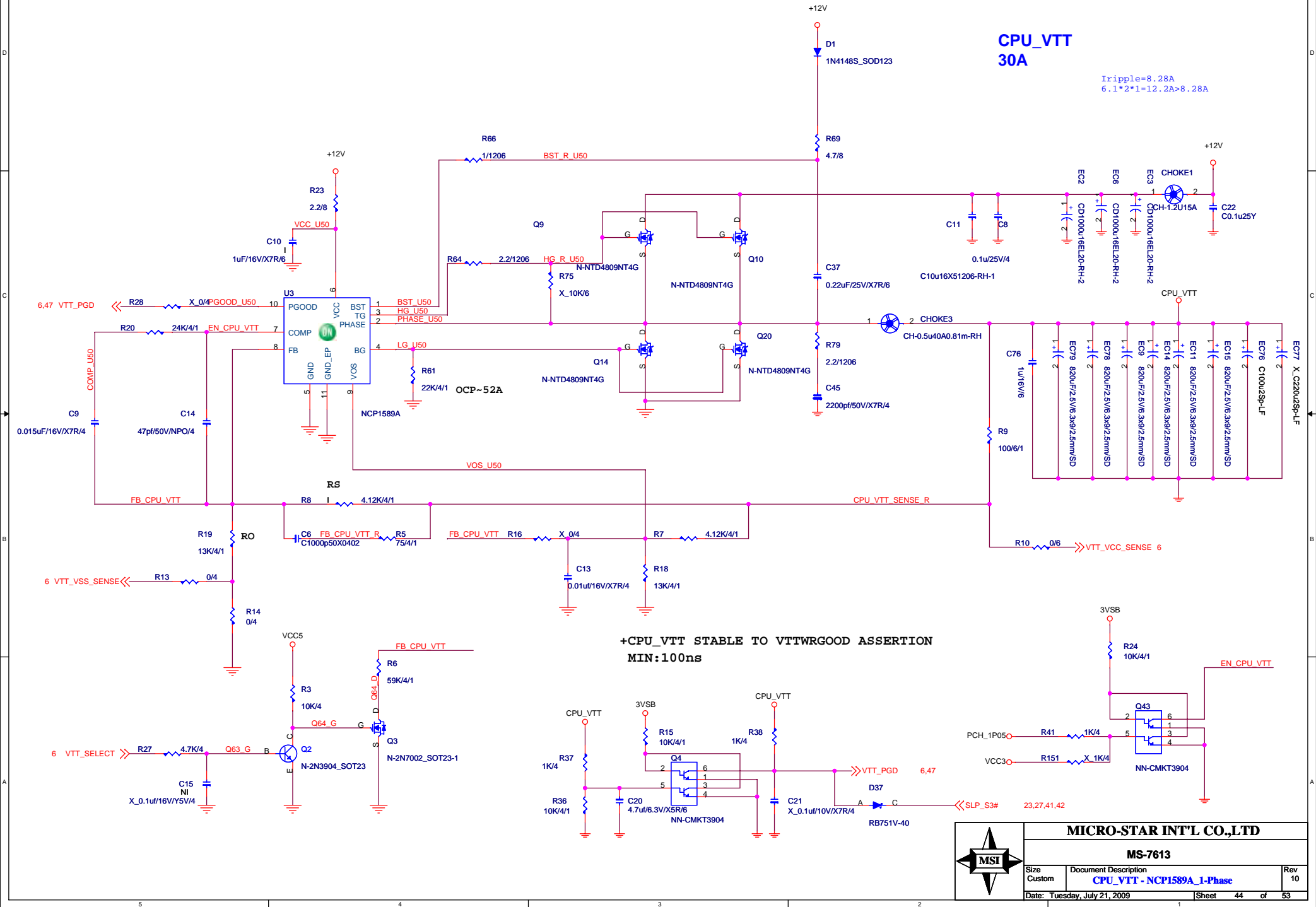
MICRO-STAR INT'L CO.,LTD

MS-7613

Size Custom Document Description **DDR POWER - UPI6103_1-Phase** Rev 10

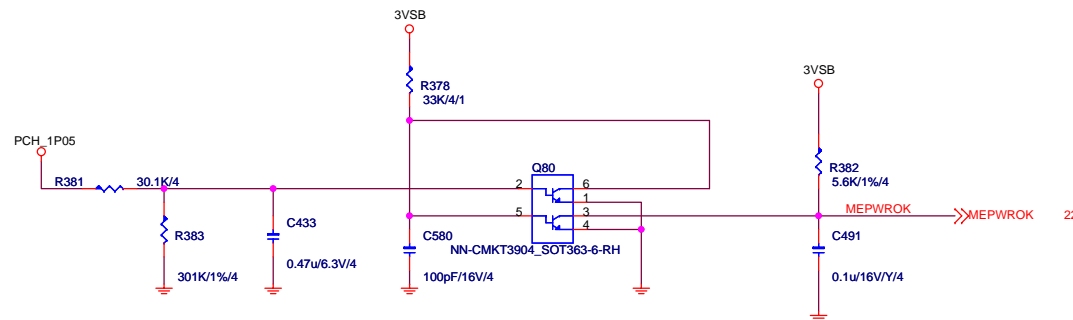
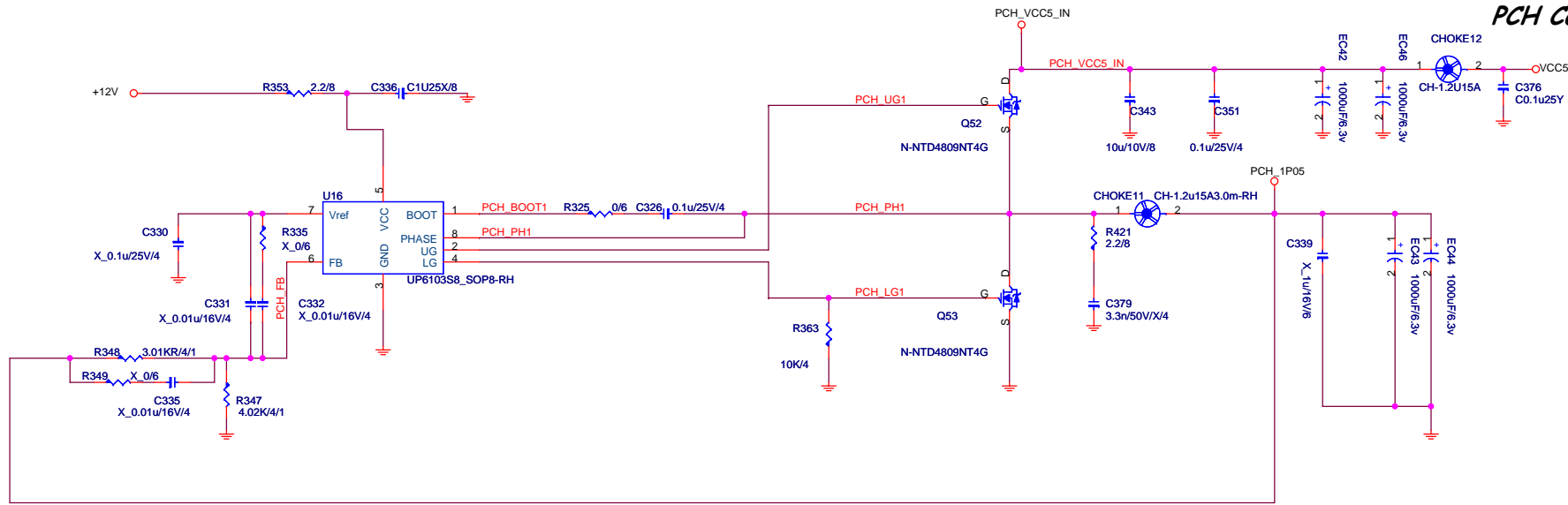
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VTTWRGD LEVEL SHIFT

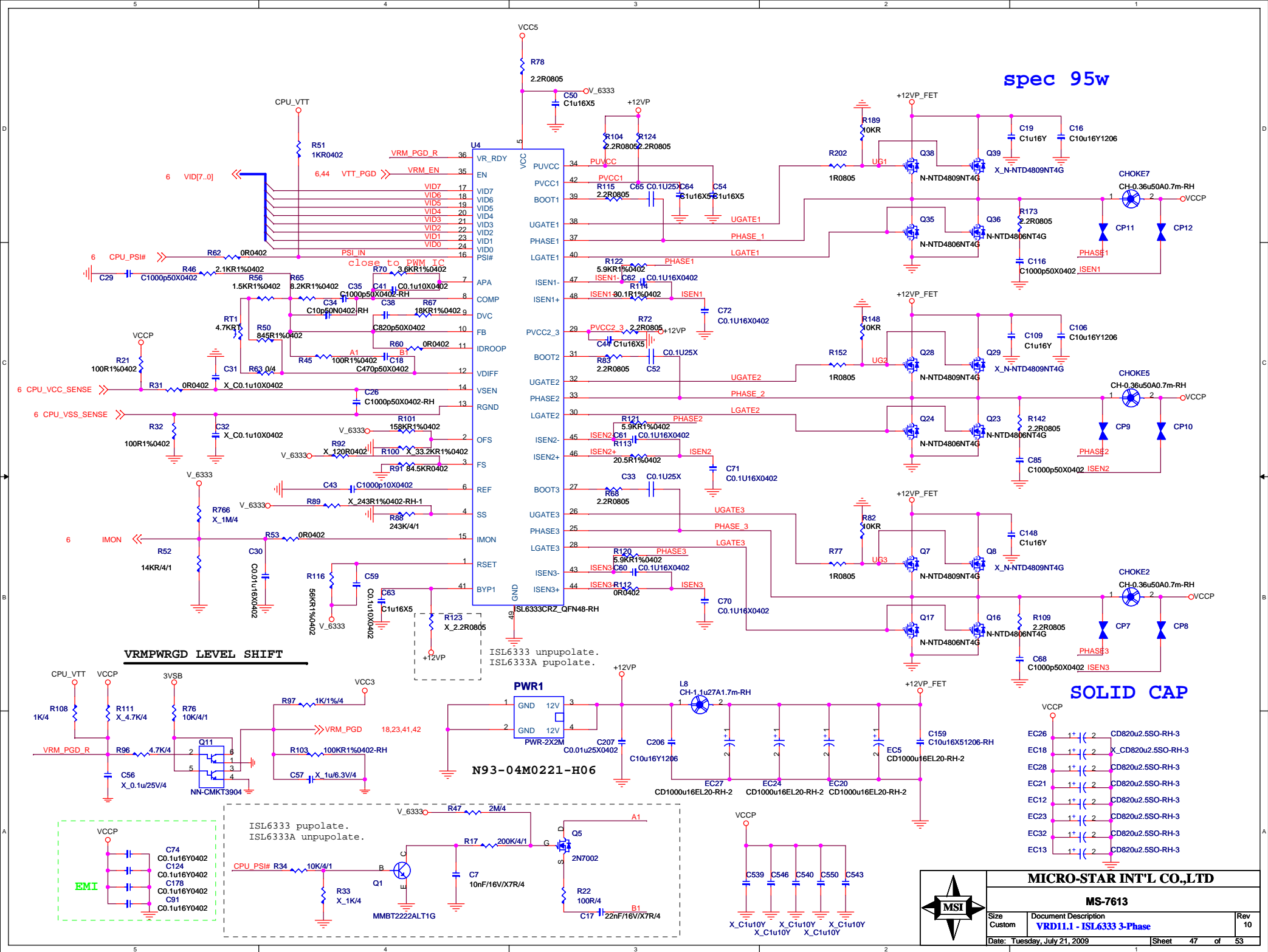


5.5A+2.5A(VCCME)=8A

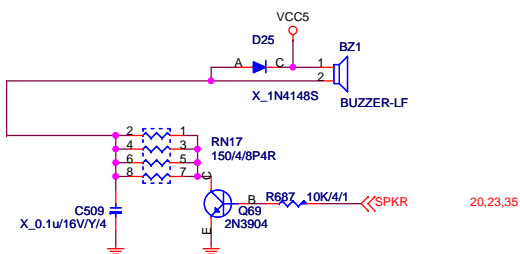
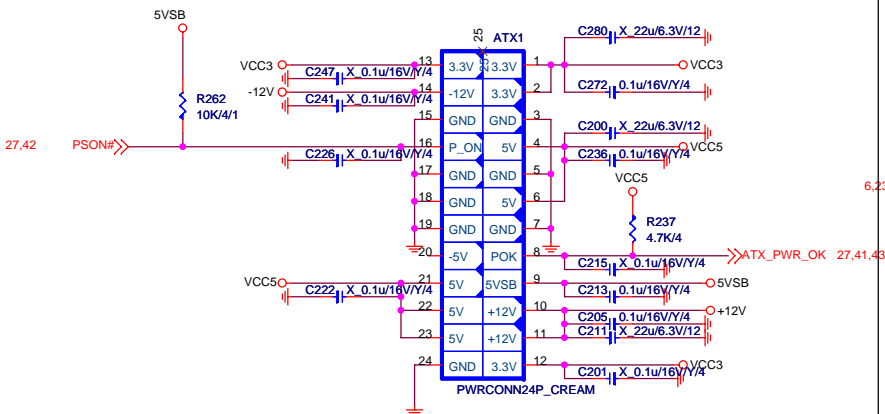
PCH Core



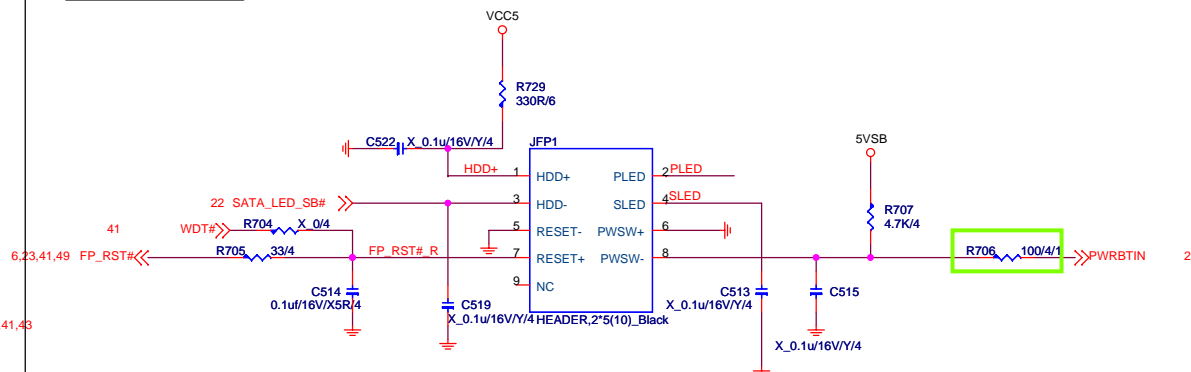
MICRO-STAR INT'L CO.,LTD			
MS-7613			
Size	Document Description		Rev
Custom	PCH POWER - UPI6103_1-Phase		10
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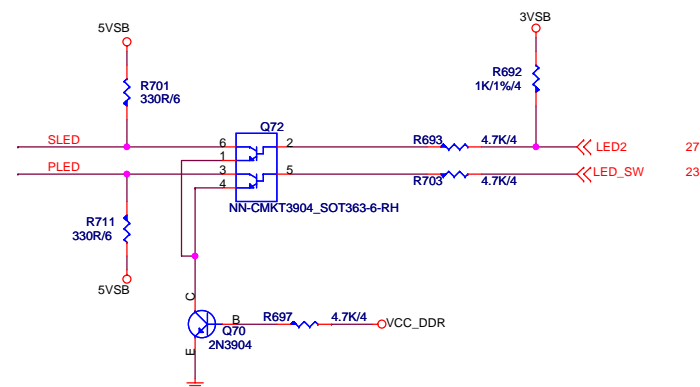
ATX POWER CONNECTOR



FRONT PANNEL



LED



	Single color LED		Dual color LED	
	LED2	LED_SW	LED2	LED_SW
S0	H	L	H	L
S1/S3	Blinking	L	L	H
S4/S5	L	L	L	L

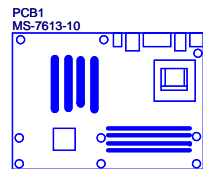


MICRO-STAR INT'L CO.,LTD

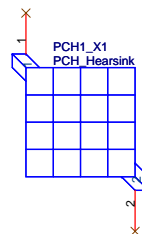
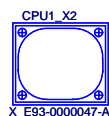
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Custom	ATX PWR-Connector/LED	10
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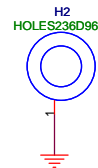
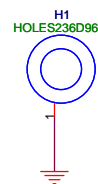
PCB



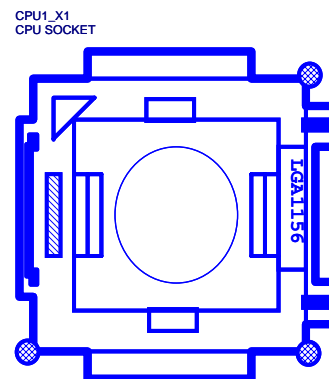
P30-0761310-G37



E31-0401634-K08

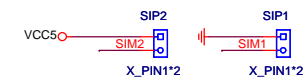


CPU SOCKET

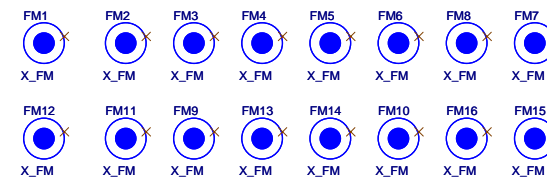


E21-7557010-F02

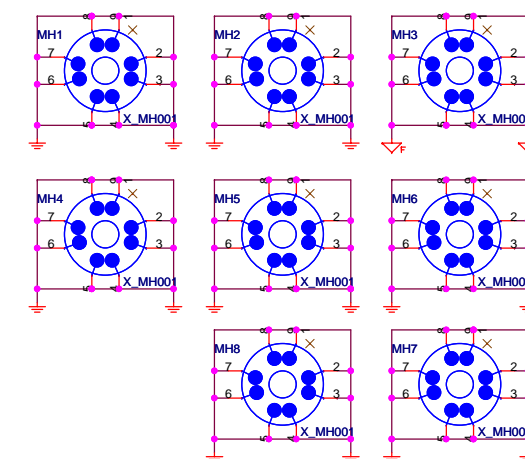
Simulation



Optical Fiducial Marks-120



Mounting Holes



ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

CPU PW
12V
+/-5%

VRD11.1
+CPU_VCCP
PWM
REGULATOR

+CPU_GFX
(Havendale
Only) PWM
REGULATOR

+CPU_VTT PWM
REGULATOR

5V_DIMM Linear
REGULATOR

VCC_DDR PWM
REGULATOR

PCH_1P05 PWM
REGULATOR

5V_USB Linear
REGULATOR

3VSB Linear
REGULATOR

X1 PCIE per
+3.3V 3.0A
+12V 0.5A
+3.3Vaux 0.4A

X16 PCIE
+3.3V 3.0A
+12V 5.5A
+3.3Vaux 0.4A

USB X8 FR
VDD
5V_USB
4.0A

USB X6 RL
VDD
5V_USB
3.0A

HAVENDALE/LYNNFIELD (95W
VCCP (CPU core 8 bit VID) 80A
VAXG (GFX core) 15A
VTT (CPU Uncore, I/O) 30A
VccPLL (SFR supplies <0.8A)
VDDQ (DDR I/O) 2.8A

PCH Ibex Peak (5.5W)
V_CPU_IO 1.05V 33uA
V5REF 5V 2.4uA
V5REF_Sus 5V 6uA
Vcc3_3 3.3V 0.3572A
VccAClk 1.05V 0.034A
VccADAC 3.3V 0.0691A
VccADPLL 1.05V 0.0782A
VccADPLLB 1.05V 0.0782A
VccCore 1.05V 1.7481A
VccDMI 1.05V 0.0655A
VccIO 1.05V 3.4059A
VccLAN 1.05V 0.4002A
VccME 1.05V 2.4072A
VccME3_3 3.3V 0.0862A
VccPNAND 1.8V 0.1559A
VccRTC 3.3V 0.0022A
VccSus3_3 3.3V 0.1680A
VccSusHDA 3.3V 0.0060A
VccVRM 1.8/1.5V 0.1829A
VccAPLLEXP 1.05V 0.045A
VccFDIPLL 1.05V 6mA
VccSATAPLL 1.05V 0.032A

HD Audio ALC888S-VC2
+5VR 51 mA
VCC3 40 mA

LAN RTL8111DL
VDD3 58mA
VDD1P2 289mA



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Power Delivery		
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Version 0A:

2009/03/16
Page 23: Populate R668 by Intel suggestion.
Page 23: Populate 100k ohm in R668 by Intel suggestion.
Page 23: Unpopulate R214 by Intel suggestion.

Version 0B:

2009/03/17
Page 35: Add internal amplifier circuit by HP requestion.
Page 34: Remove internal line-in circuit by HP requestion.
Page 6: Add CPU POC circuit following Design guide..
Page 47: Change R123 to 2.2ohm/0805 reserve for ISL6333A.
Page 39: Change USB port 0, 1 OC from OC#5 to OC#0 following Design guide.
Page 36: Change R143 and R140 from 100 ohm to 0 ohm by Intel suggestion.
Page 23: Pull-up GPIO57 to 3VSB by Intel suggestion.
Page 23: Unpopulate R603 by Intel suggestion.
Page 23: Pull-up SML0CLK and SML0DATA to 3VSB by Intel recommend.
Page 23: Pull-up SMBCLK and SMBDATA to 3VSB by Intel recommend.
Page 23: Swap HAD_SYNC and HAD_RST to match ball name.
Page 23: Connect PCH_JTAGRST# to a test point by Intel recommend.
Page 49: Connect SATA4GP to Pin 34 of the JTAG connector by Intel recommend.
Page 49: Connect Pin 41 of the JTAG connector to a test point by Intel recommend.
Page 49: Connect VCC of the JTAG connector to 3VSB by Intel recommend.
Page 23: Connect GIOP26 to control audio de-pop circuit.
Page 23: Use GIOPI3 to switch audio Verb Table with internal amplifier or not.
Page 37: Reserve R512 for DVI level shifter eable control.
2009/03/19
Page 20: Change R539 and R546 from 39 ohm to 22 ohm by Intel recommend.
Page 27: Reserve R766 for RSMRST# timing control.
Page 23: Change GPIO45, GPIO46, GPIO47 pull-up well from VCC3 to 3VBS following schematic checklist.
Page 22: Connect SATA port4 to SATA5 connector by HP recommend.
Page 22: Connect SATA port2 to SATA3 connector by HP recommend.
Page 22: Use GPIO22, GPIO38, GPIO39, GPIO48 for MB_ID.
Page 32: Unpopulate C216 for EEPROM can not be programed issue.
2009/03/20
Page 42: Reserve discharge circuit.
Page 47: Connect IMON pin of VRD to ISENSE of CPU.
2009/03/23
Page 32: Unpopulate C209, C210, C214 to fix LAN LED wrong.
Page 42: Add R771 approve VCC1_5 whitout load.
2009/03/24
Page 22: Delete SATA5, SATA6 connector.
Page 22: Change SATA1 and SATA2 to right angle connector.
Page 15: Change C160 to 22uF/0805 and add a 22uF/0805 in C470.

2009/03/25
Page 23: Change R595 from 10k ohm to 1k ohm.
Page 23: Reserve R561 to pull-up FP_RST# to 3VSB.
Page 30: Add R813 and R814 to switch Mini-card support wake function or not.
Page 41: Change R650 from 4.7k ohm to 1k ohm for approving CHIP_PWGD signal level.
2009/03/26
Page 34: Move D24 to pin2 of U27.
Page 34: Change R681 from 309 ohm to 324 ohm.
Page 34: Connect D32 to 3VSB.
Page 30: Add Wireless LED (JWLED) by HP requirement.

2009/03/27

Power solution:

Page 47: Change R50 from 681 ohm to 931 ohm.
Page 47: Change R56 from 1.24k ohm to 1.33k ohm.
Page 47: Change R101 from 162k ohm to 255k ohm.
Page 47: Change C34 from 33 pF to 10 pF.
Page 47: Change C35 from 470 pF to 1000 pF.
Page 47: Change R65 from 16.5k ohm to 21k ohm.
Page 47: Change R70 from 5.1k ohm to 3k ohm.
Page 12: Populate C96 and C98.
Page 47: Populate 4700pF cap in C29 and 2.49k ohm resistor in R46.
Page 47: Change R52 from 13.3k ohm to 14.3k ohm.
Page 47: Change CHOKE2, CHOKE5 and CHOKE from 0.5uH to 0.36uH
Page 47: Populate EC32.
Page 47: Change R120, 121 and R122 from 6.19k ohm to 5.11k ohm.
Page 44: Change C6 from 0.015uF to 4700pF.
Page 44: Change R8 from 4.32k ohm to 4.12k ohm.
Page 44: Populate 820uF cap in EC78.
Page 44: Change EC76 from 100uF to 220uF and non-stuff EC77.
Page 44: Add a 820uF cap in EC79.

2009/03/30

Page 23: Change R642 from 4.75k ohm to 1.1k ohm.
and R641 from 12.1k ohm to 3k ohm following Intel MOW WW13 2009.
Page 27: Change R571 from 5.6k ohm to 5.9k ohm to meet RSMRST# falling spec.
and unpopulate C456 to meet RSMRST# falling spec.

2009/03/31

Page 20: Reserve C471, C479 and C483 for EMI.

2009/04/02

Page 26: Un-stuff R431 and R400.
Stuff R423, R401, R367, R475, R371 and R450 for using external LC filter.
Page 38: Connect Pin 1 of U1 to fix system fan always full on.
Page 48:Use GPIO31 to control power LED for LED turn red then green with dual color LED.

2009/04/06

Page 33: Reserve C485 for AZ_SDOUT.

2009/04/07

Page 34: Reserve Q78, Q79, R773, C475, R702, R773 for power saving in S5.
Page 43: Change R200 from 1.3k ohm to 1.33k ohm for DDR power quality.
Page 27: Add D36 and connect to ATX_PWR_OK for AC power lost last state function adnormal.
2009/04/09

Page 18: Change Clock gen from realtek RTM875N-606 to realtek RTM885N-932.
Page 44: Add D37 to fix CPU_VTT leakage in S3 state.



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Version 0C:

2009/04/21

Page 23: Reserve C365 to fix sometime the system auto wake when insert PCIE device.

Page 27: Connect KBRST# and A20GATE of IO to PCH KBRST# and A20GATE.

Page 23: Use GPIO44 to control onboard LAN power.

2009/04/27

Page 28: Add C412 for PCIE slot power.

Page 34: Reserve C419 for audio power.

2009/05/06

Page 40: Leave pin10 of JUSB1 and JUSB2 NC for some card reader work abnormal.

Page 41: Change EC67 to 1000uF for 3VSB power quality.

Page 37: Swap DVI_TXD2+ and DVI_TXD2-.

2009/05/07

Power Solution:

- Page 12: Unpopulate C146, C139, C181
- Page 12: Unpopulate C142, C155, C168, C171, C179, C176, C167, C145
- Page 44: Change EC76 from 220uF to 100uF.
- Page 44: Change C6 from 4700pF to 1000pF.
- Page 47: Change R101 from 255k ohm to 158k ohm.
- Page 47: Change C18 from 680 pF to 470pF.
- Page 47: Change R70 from 3k ohm to 2.74k ohm.
- Page 47: Change R120, R121 and R122 from 5.1k ohm to 5.9k ohm.
- Page 47: Change C29 from 4700 pF to 1000pF.
- Page 47: Change R46 from 2.49k ohm to 2.1k ohm.
- Page 47: Change R45 from 750 ohm to 100 ohm.
- Page 47: Change R65 from 2.1k ohm to 8.2k ohm.
- Page 47: Change C35 from 1000 pF to 3300pF.
- Page 47: Change R52 from 14.3k ohm to 14k ohm.
- Page 47: Change R56 from 1.33k ohm to 1.4k ohm.
- Page 46: Change R290 from 9.1k ohm to 15.4k ohm.
- Page 46: Change R309 from 19.6k ohm to 23.7k ohm.
- Page 46: Change R286 from 100k ohm to 82k ohm.

2009/05/11

Page 18: Change clock gen from RTM885N-932 to Silego SLG8SP585

Page 27: Change R571 from 5.9K ohm to 5.6K ohm for meet RSMRST# falling time.

Page 12: Populate 0 ohm in C186 following WW16 MoW

(Discrete graphic only support, VAXG tie to GND)

Page 11: Populate R293, R299 following WW18 MoW

Page 30: Connect LED_WLED to pin4 of JWLED for meet LED cable define.

Page 22: Change SATA1 and SATA2 connector type to DIP.

2009/05/18

Page 23: Change C495 and C500 from 10pF to 18pF.

Page 13, 15: Change C137 and C161 from 0.1uF to 2.2uF to improve Vref_CA power.

Page 30: Reserve R780 for mini card.

Page 30: Connect R813 to 3VSB_SLOT.

Page 21: Add R375 and R376 for support two TL-399.

2009/05/26

Page 23: Populate R619 to fix TV tuner card can't be detected when system restart.

2009/06/16

Power Solution:

Page 46: Un-stuff R33.

Page 46: Change R50 from 931 ohm to 845 ohm.

Page 46: Change R56 from 1.4K ohm to 1.5K ohm.

Page 46: Change R70 from 2.74K ohm to 3.6K ohm.

Page 46: Change C35 from 3300 pF to 1000 pF.

Page 46: Stuff 1000 pF in C26.

Page 44: Change R6 from 69.8K ohm to 59K ohm.

2009/06/22

Page 24: Un-stuff C560

Page 24: Change C557 to 0 ohm.

2009/06/25

Page 39: Change R216,R212,R40,R733,R715,R719,R732 from 220 ohm to 10K ohm.

Page 39: Change R217,R213,R59,R723,R710,R708,R723 from 330 ohm to 15K ohm.

Version 0D:

2009/06/22

Page 45: Add MEPWRGD circuit.

2009/06/25

Page 23: Add RECOVERY header.

2009/06/26

Page 37: Reserve C581 for EMI.

2009/06/30

Page 20: Reserve R393 and R395.

2009/07/02

Page 42: Reserver C582 and C583 for EMI.

Page 49: Reserve R545,R782,R783 and R784.

2009/07/09

Page 49: Un-stuff R579,R558,R543,R584,R568,R534.

2009/07/14


Power Solution:

Page 44: Un-stuff R16.

Page 44: Stuff 4.12k ohm in R7.

Page 44: Stuff 13k ohm in R18.

Page 44: Stuff 0.01uF in C13.

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